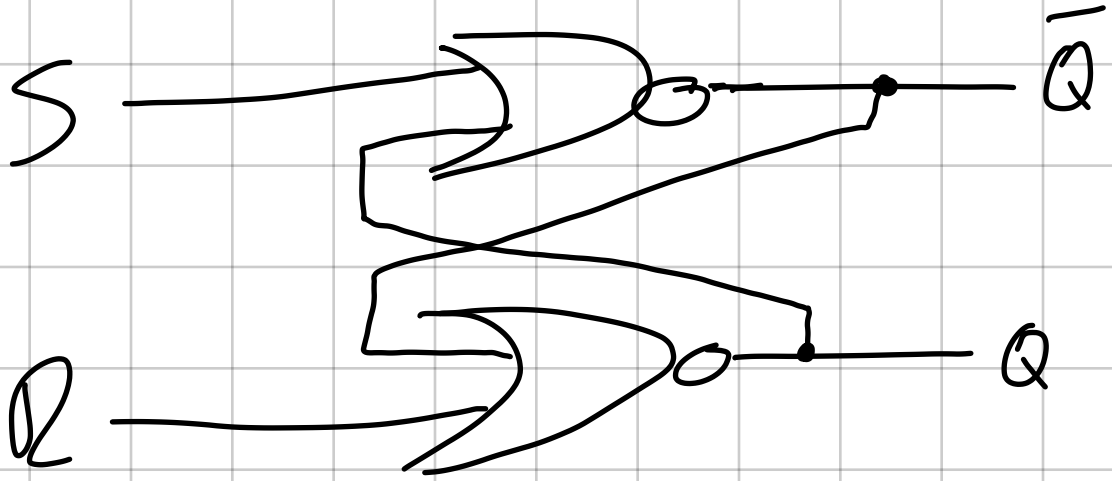
29 August 2013

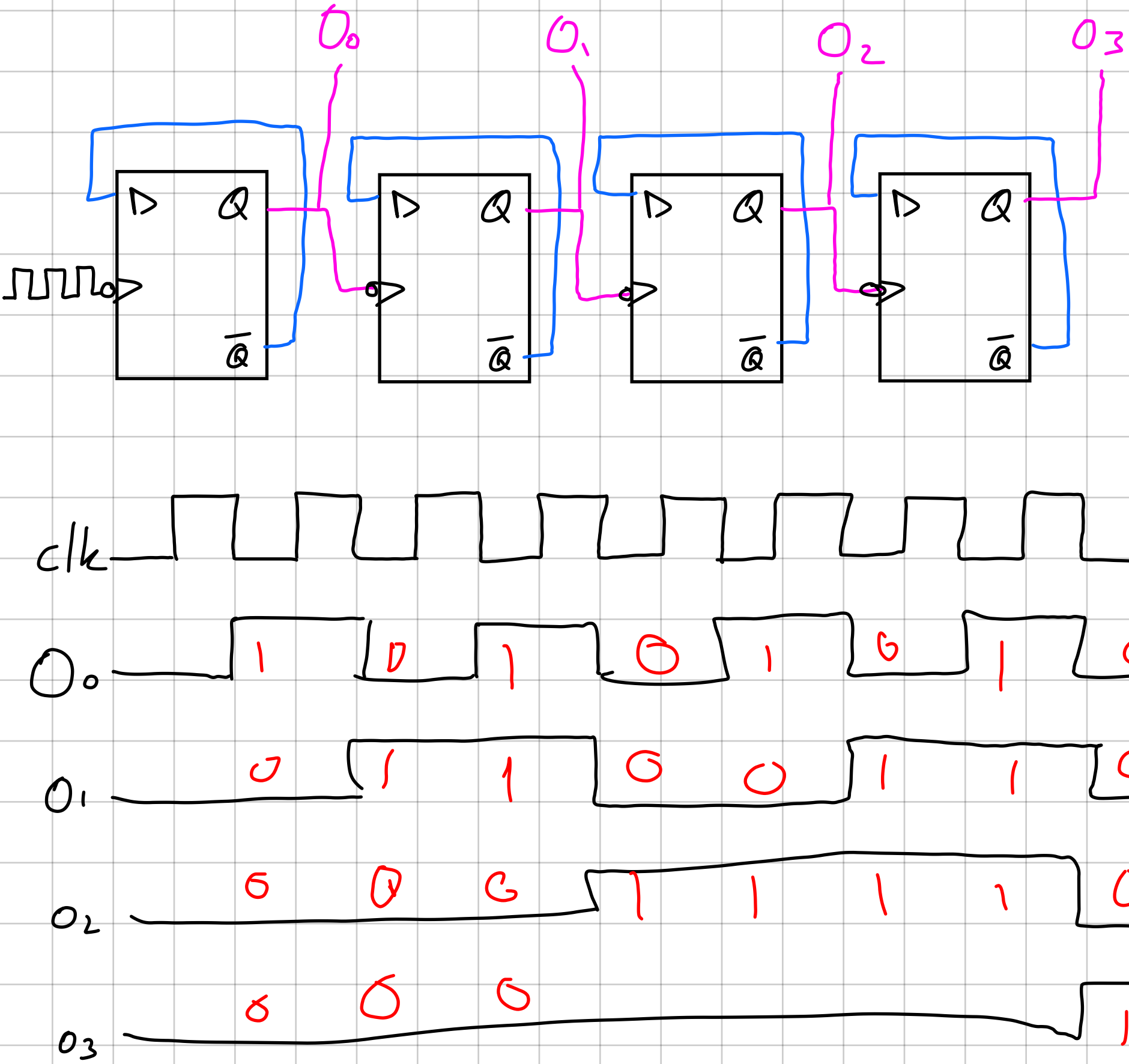
Recap: Sequential logic

- edge and level triggering
- latches vs flip-flops
- SR, JK, Master slave, D
- Timing/ triggering diagram



Must use NOR gates, if you use OR gates the latch will not work!

Ripple counter, or frequency divider!



Discussed the test process/solutions, with particular reference to question 4, HV test station