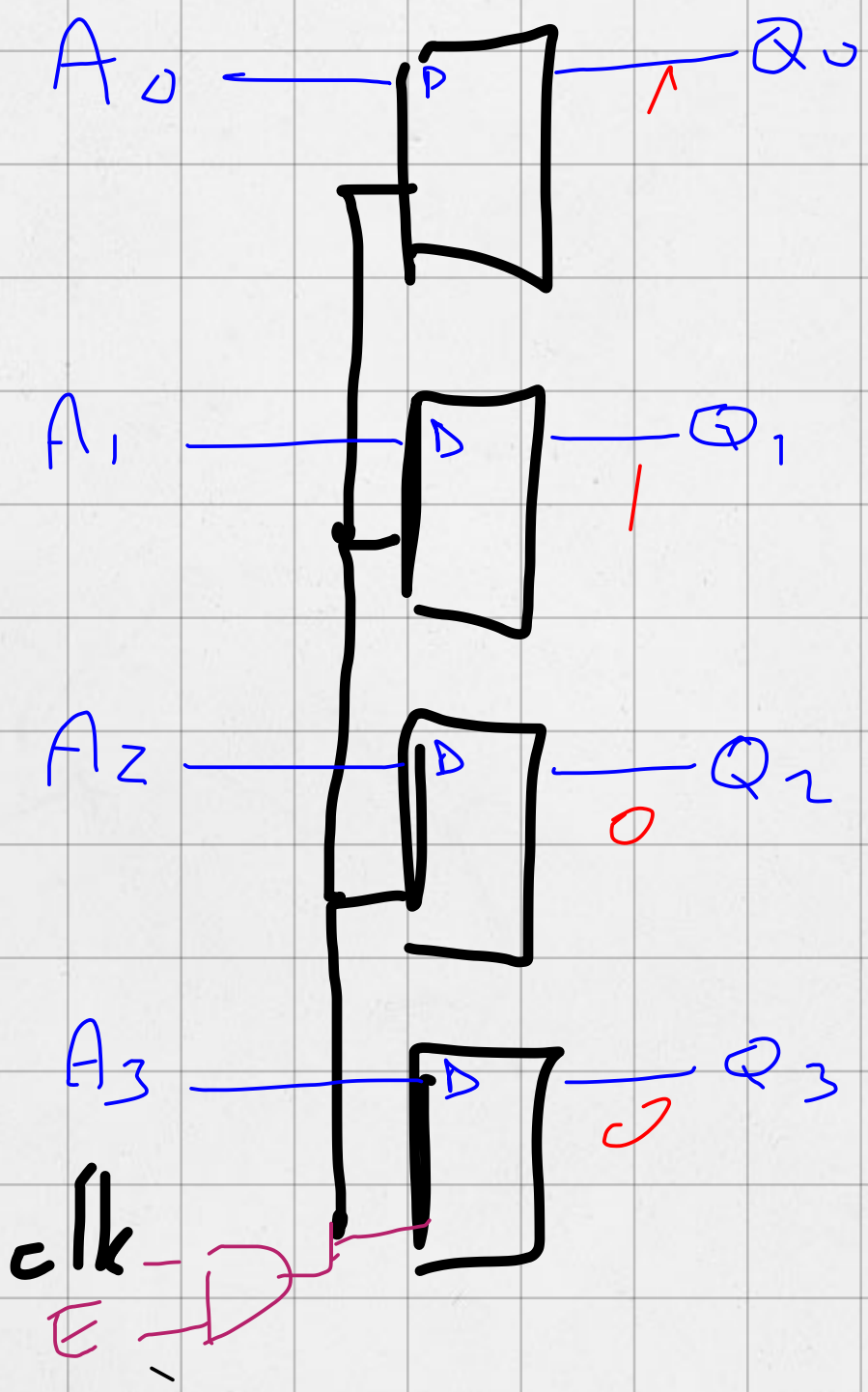
22 August 2012

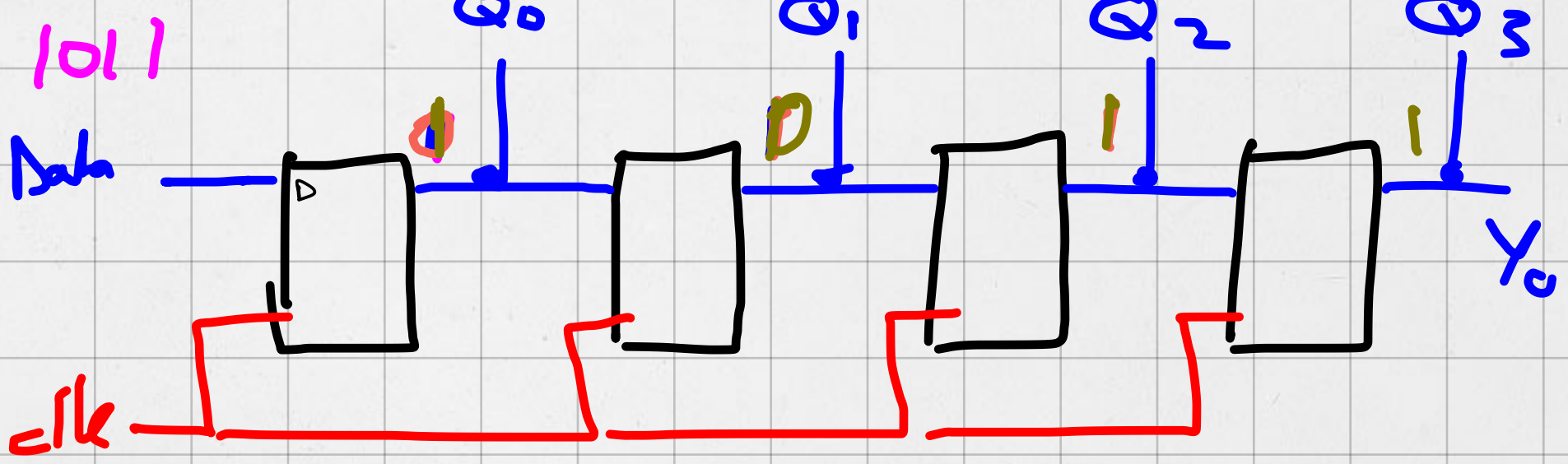


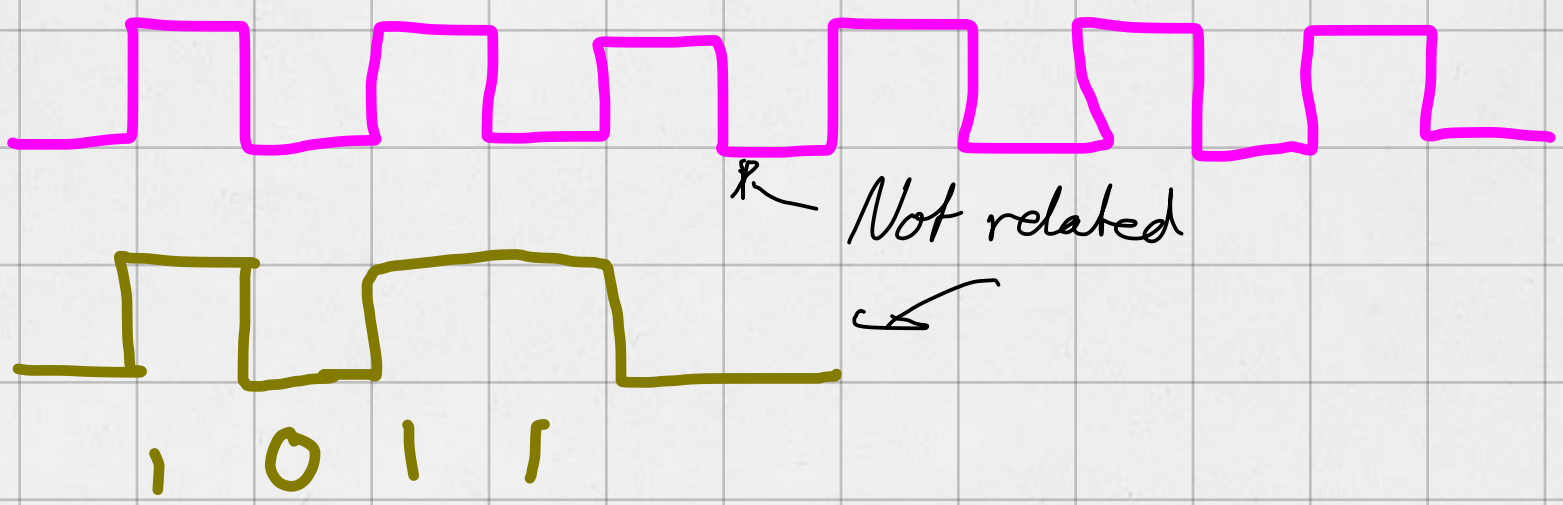
D = 1010

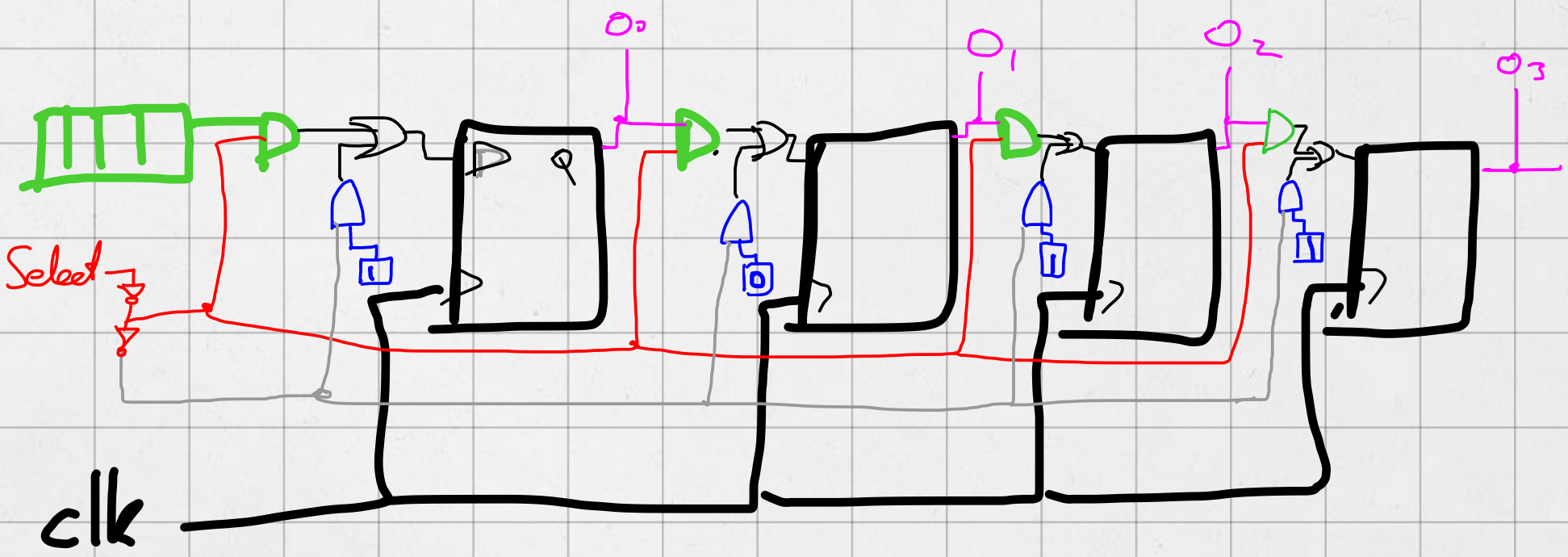
M < D

LSB.

1011

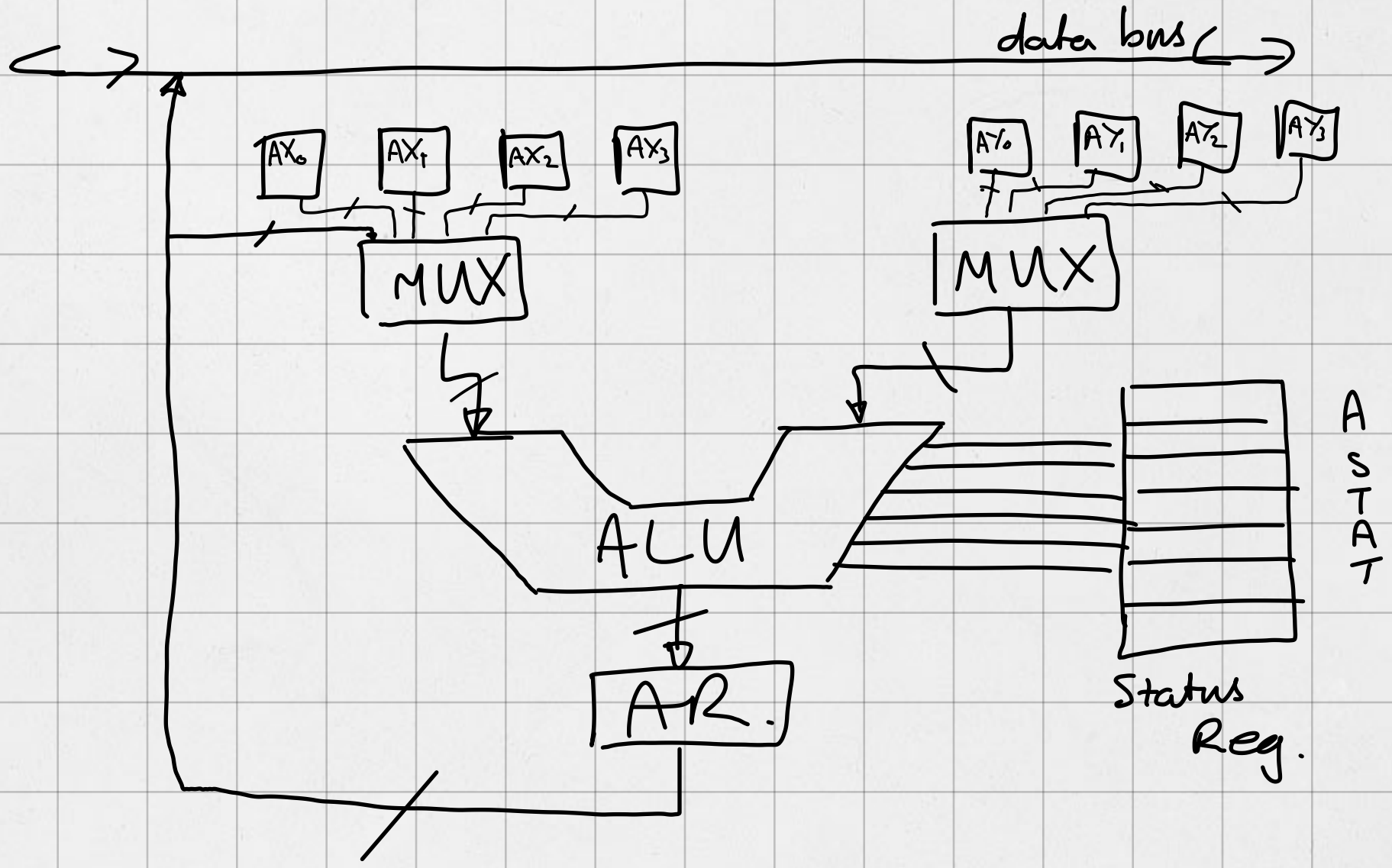


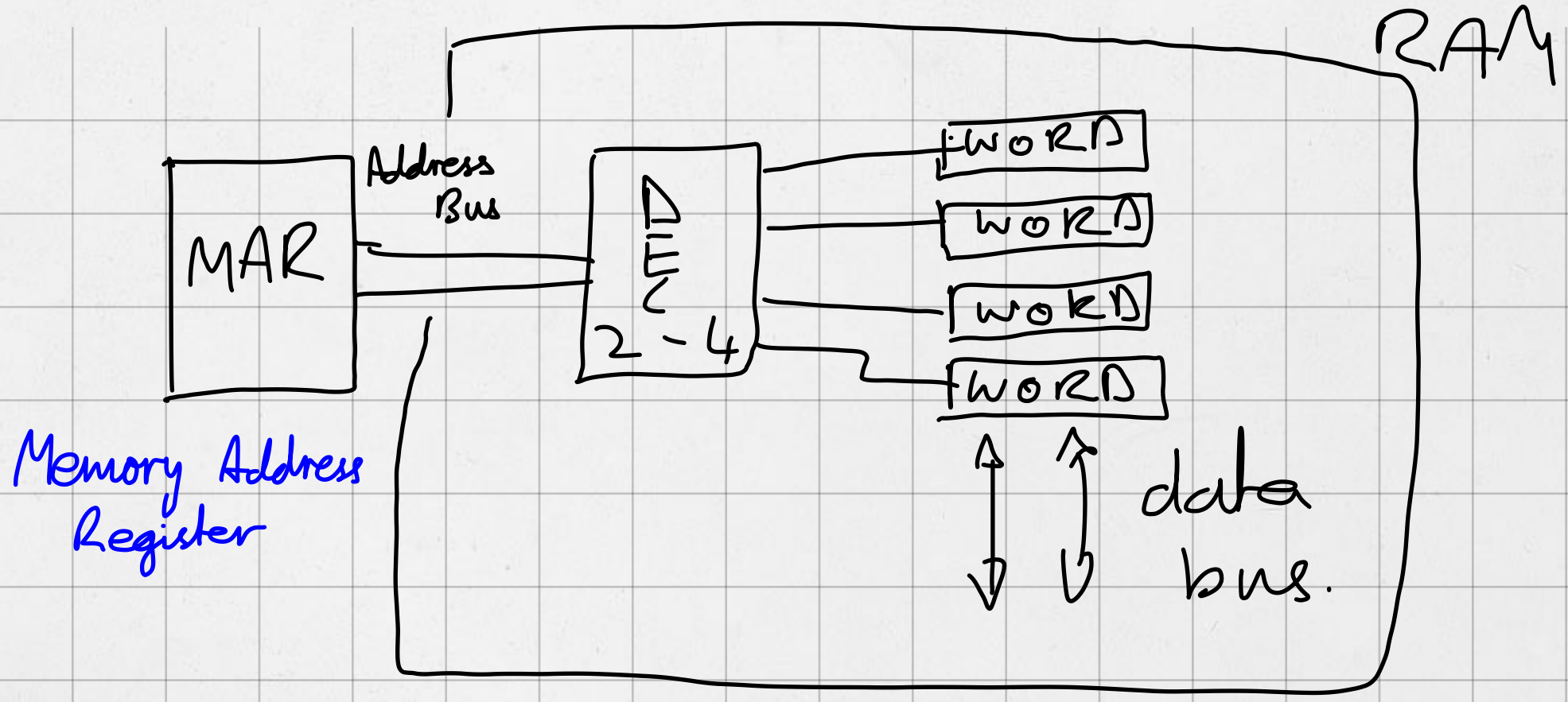


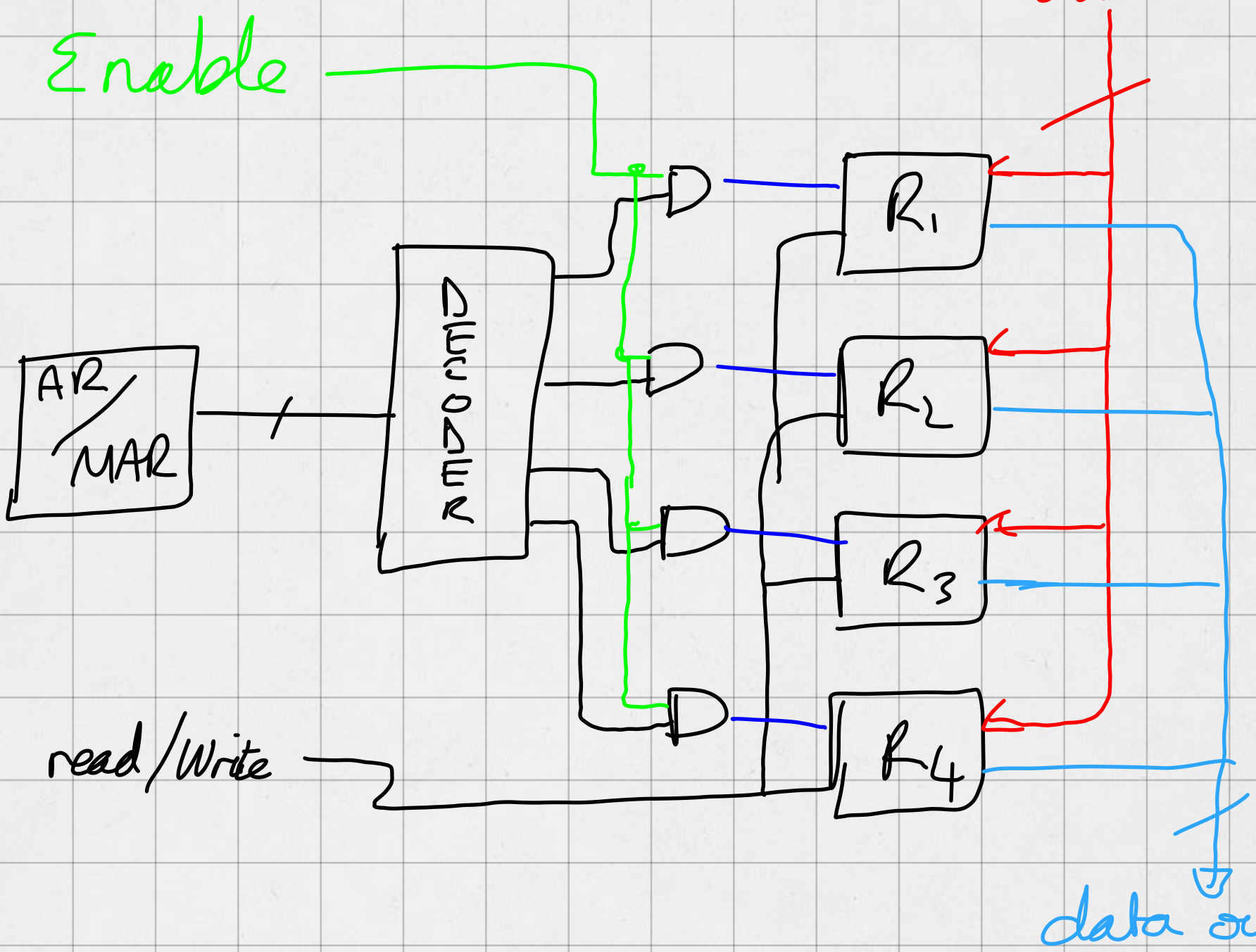

O0
O1
O2
O3
Select
clk

The next few notes were written on the black board, I have added these in just to make sure that we are all on the same page.

ALU → Arithmetic logic unit




RAM
MAR
Address Bus
DEC 2-4
WORD
WORD
WORD
WORD
data bus.
Memory Address Register


Enable
AR/MAR
DECODER
R1
R2
R3
R4
read/Write
data in
data out