Microprocessors

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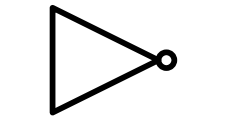
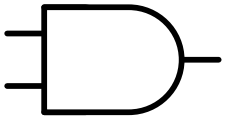
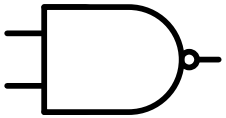
Basic building blocks - Gates



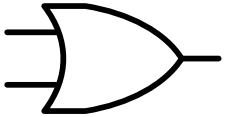
Inverter
1 ✳ 0
0 ✳ 1



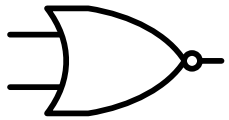
AND
0 + 0 = 0
0 + 1 = 0
1 + 0 = 0
1 + 1 = 1



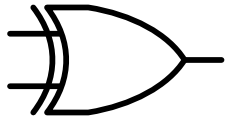
NAND
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0



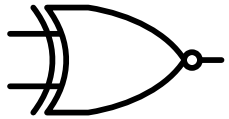
OR
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1



NOR
0 + 0 = 1
0 + 1 = 0
1 + 0 = 0
1 + 1 = 0



XOR
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0



XNOR
0 + 0 = 1
0 + 1 = 0
1 + 0 = 0
1 + 1 = 1

Boolean simplification

$$Q = \bar{A}\bar{B}C + \bar{A}BC + ABC$$

$$Q = \bar{A}C(\bar{B} + B) + BC(\bar{A} + A)$$

$$Q = \bar{A}C + BC$$

$$Q = C(\bar{A} + B)$$

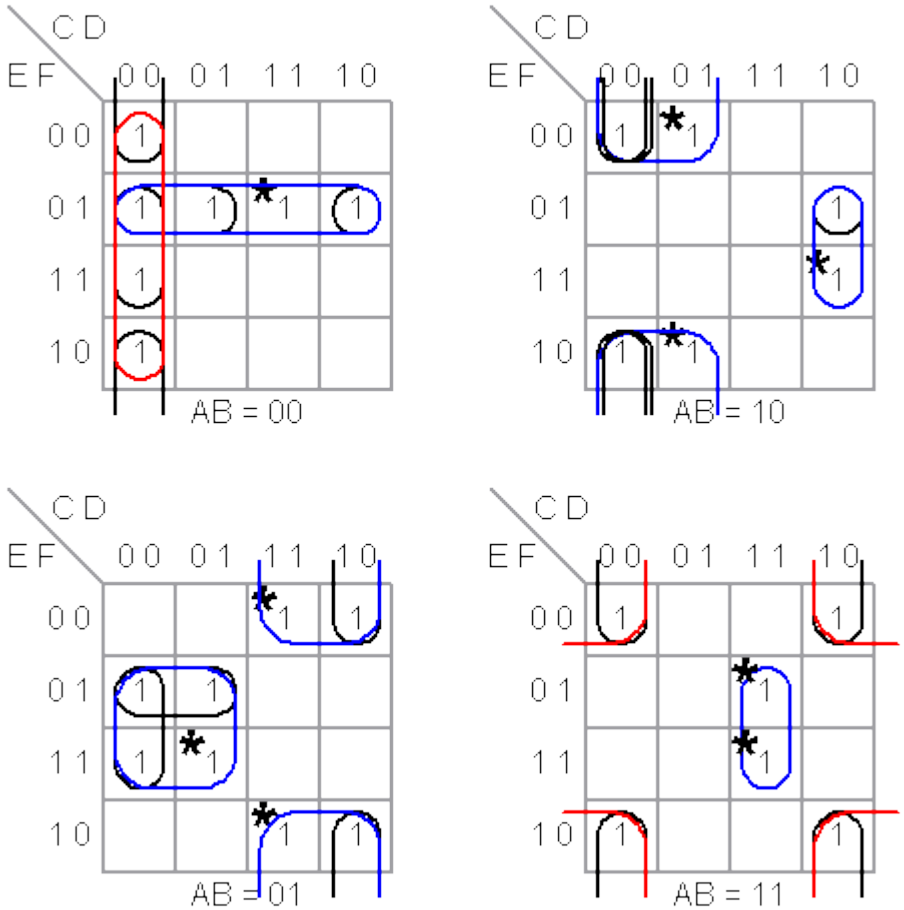
$$Q = \bar{A}C(\bar{B} + B) + ABC$$

$$Q = \bar{A}C + ABC$$

$$Q = C(\bar{A} + AB)$$

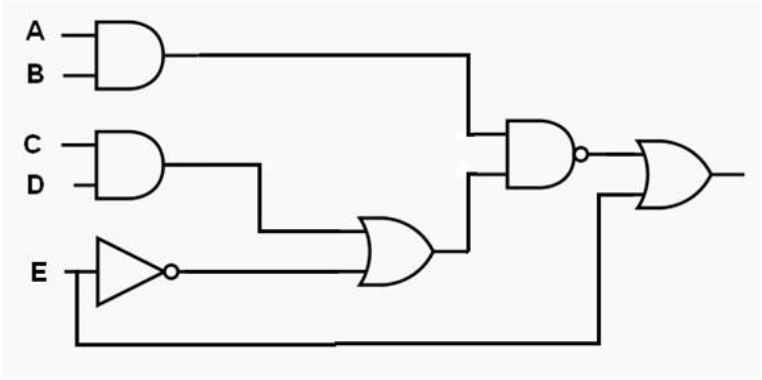
$$Q = C(\bar{A} + B)$$

Karnaugh maps

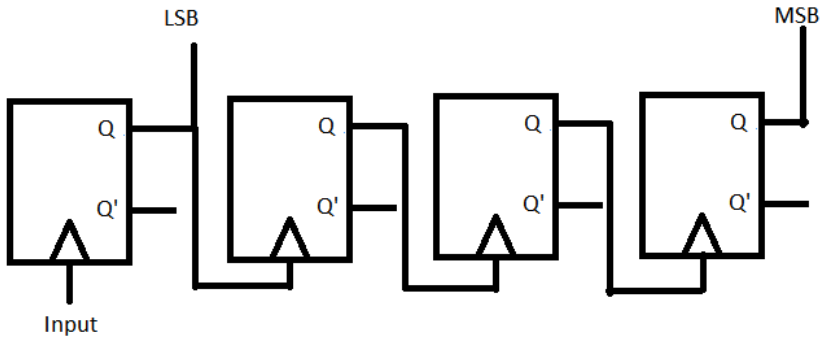


Definitions

- TTL, CMOS
- Gated Diagram –



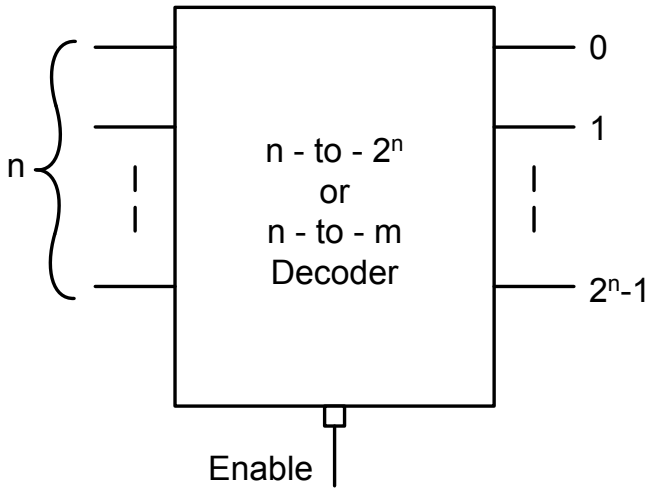
- Block diagram –



- Combinational logic
- Sequential logic

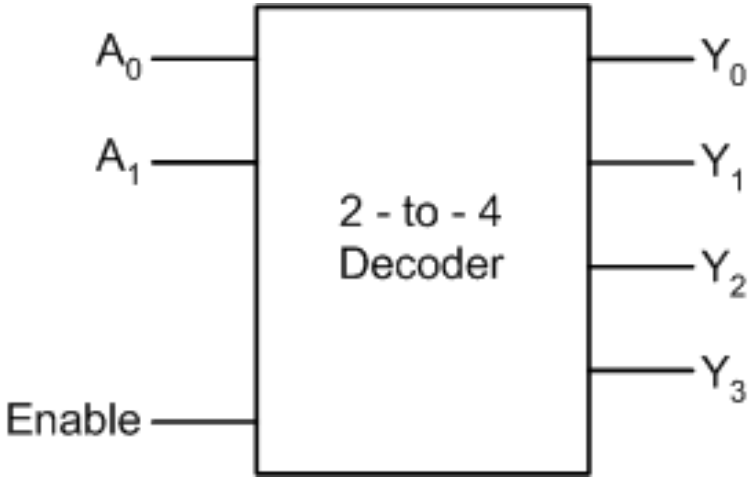
Decoders

- Device that decodes an input
- Multiple input multiple output device
- n inputs → 2^n outputs
- 2^n = m where the device is called n-to-m decoder

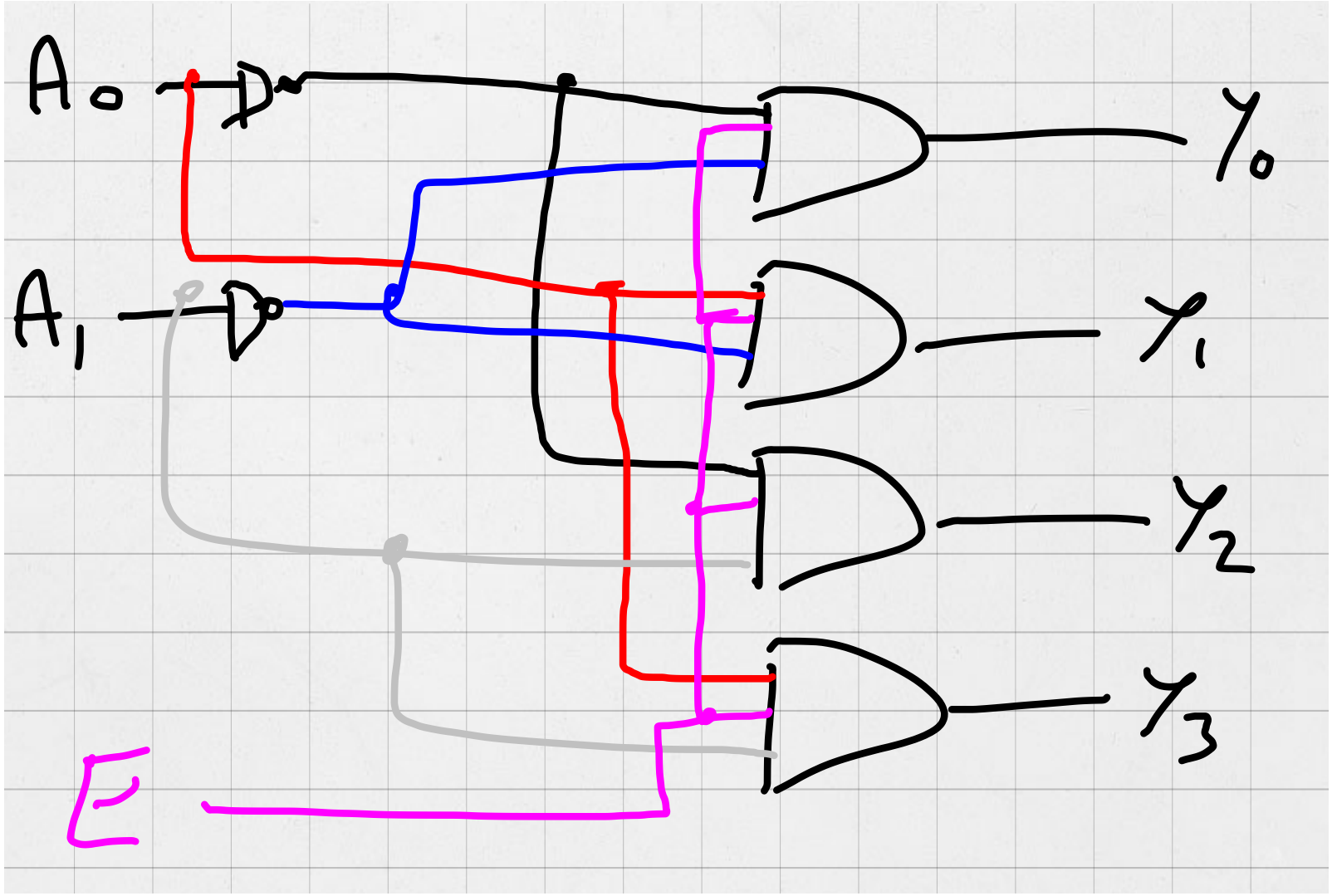


Decoder cont.

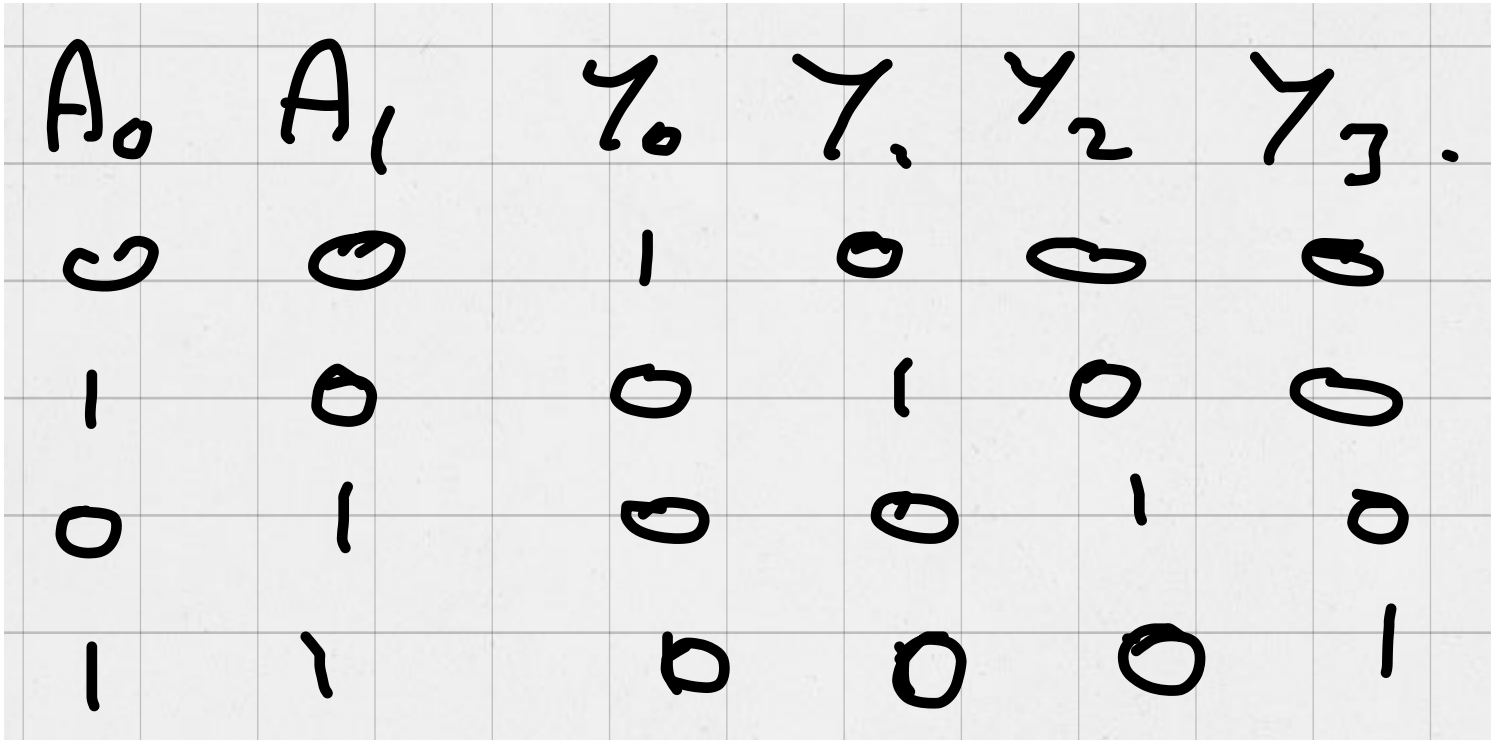
- A decoder activates exactly one of its outputs based on the input values
- Example – 2 – 4 bit decoder



Decoder cont.

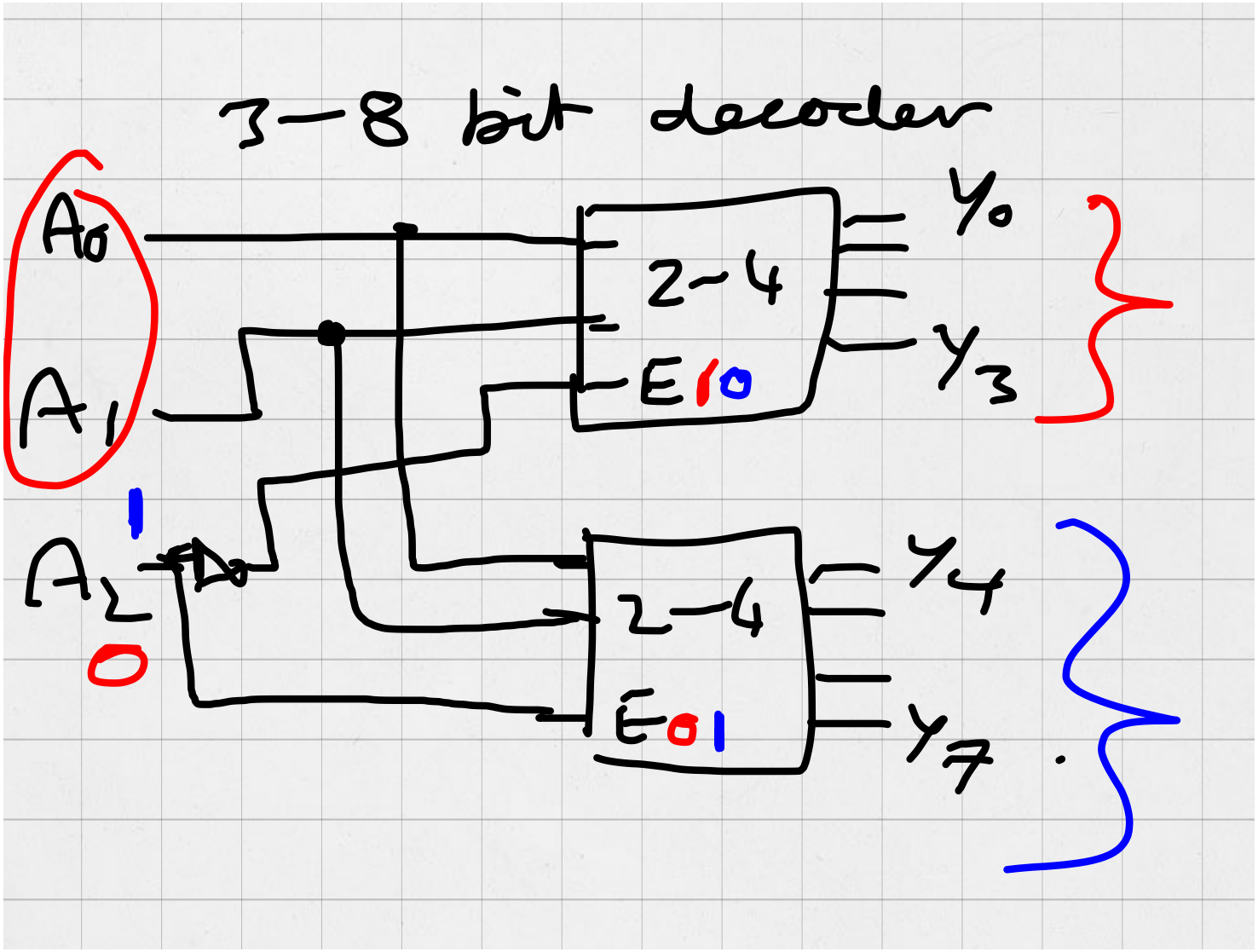


Decoder cont.



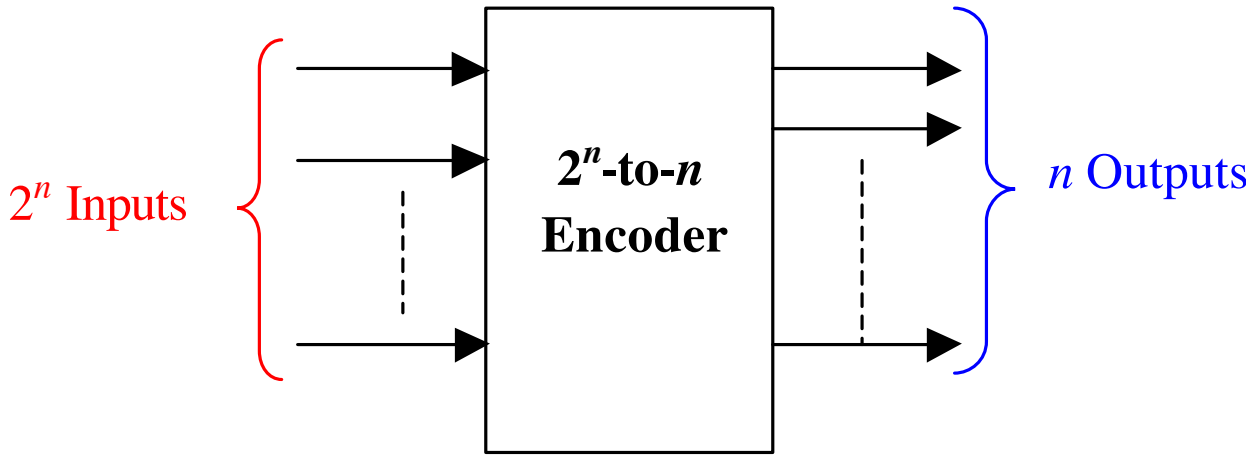
A_0	A_1	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

Decoders cont.



Encoder

- Inverse of a decoder
- 2^n inputs → n outputs
- Only 1 active high input



Encoders cont

X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1