7 September 2011

Recap:

half & full adder

4 bit -> 2 number adder

Multi-bit comparators.

NEW ⟶

Subtractor

Multipliers

Parity

A = 0110

B = 0011

A+B = 1001

0110

− 0011

0110

0011

1100

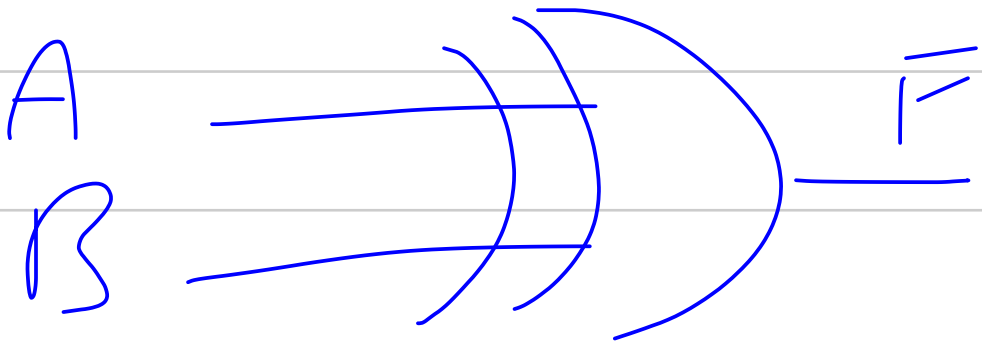
+ 0011

1101

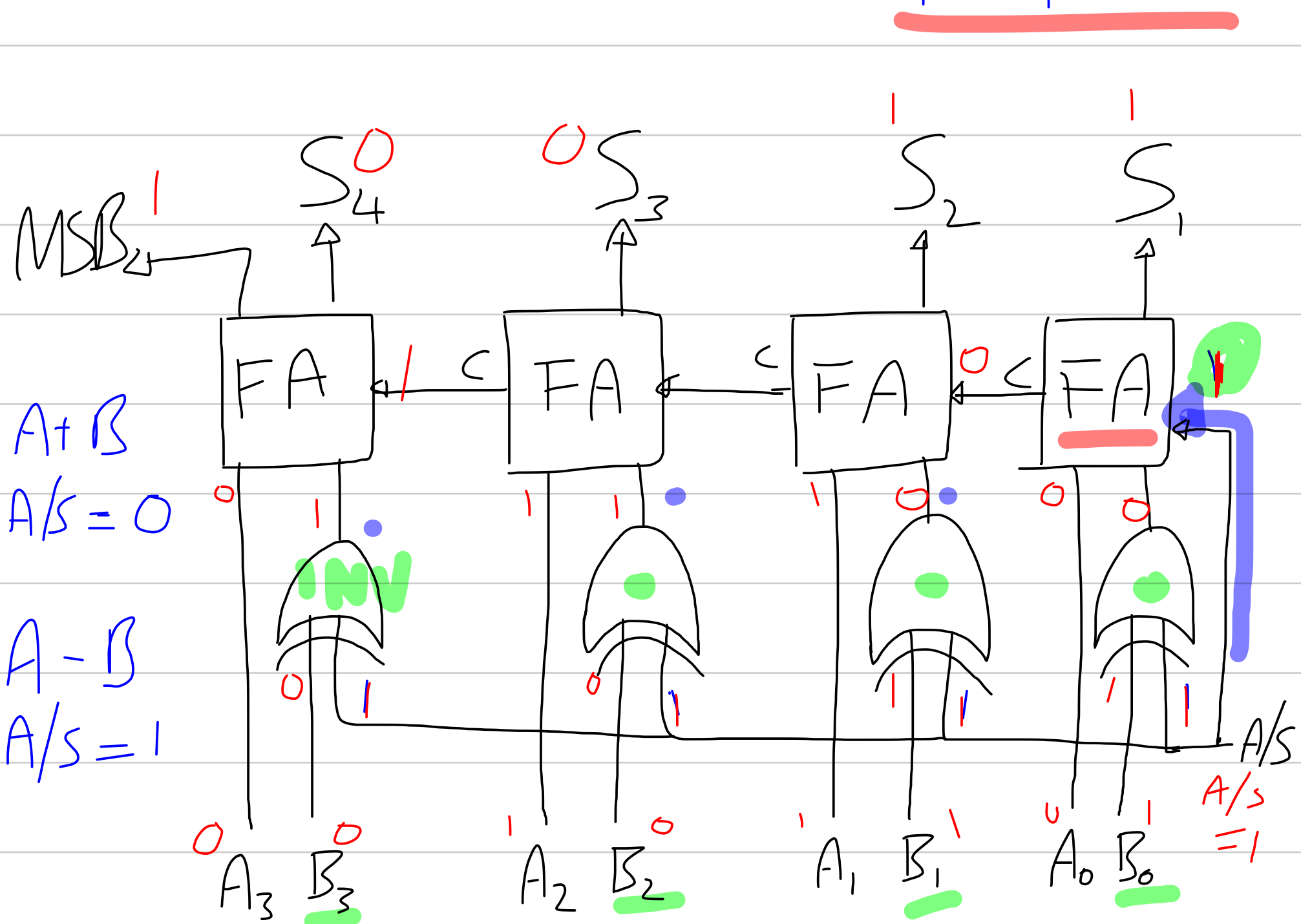
Subtractors!

2's compliment → how?

What gate component can be used?



A	B	F
0	0	0
1	0	1
0	1	1
1	1	0



Multipliers

Multiply by 2?

Repeated additions?

$$7 \times 7 = 49.$$

$$\begin{array}{r} 7 \\ +\ 7 \\ +\ 7 \\ \vdots \\ \hline 49. \end{array}$$

Numbers – A & B each two bits, how do we multiply them?

$A \Rightarrow A_1 A_0$ & $B \Rightarrow B_1, B_0$

$B_1 \quad B_0$

$A_1 \quad A_0$

$B_1 A_0 \quad B_0 A_0$

$B_1 A_1 \quad B_0 A_1$

$Y_3 \quad Y_2 \quad Y_1 \quad Y_0$

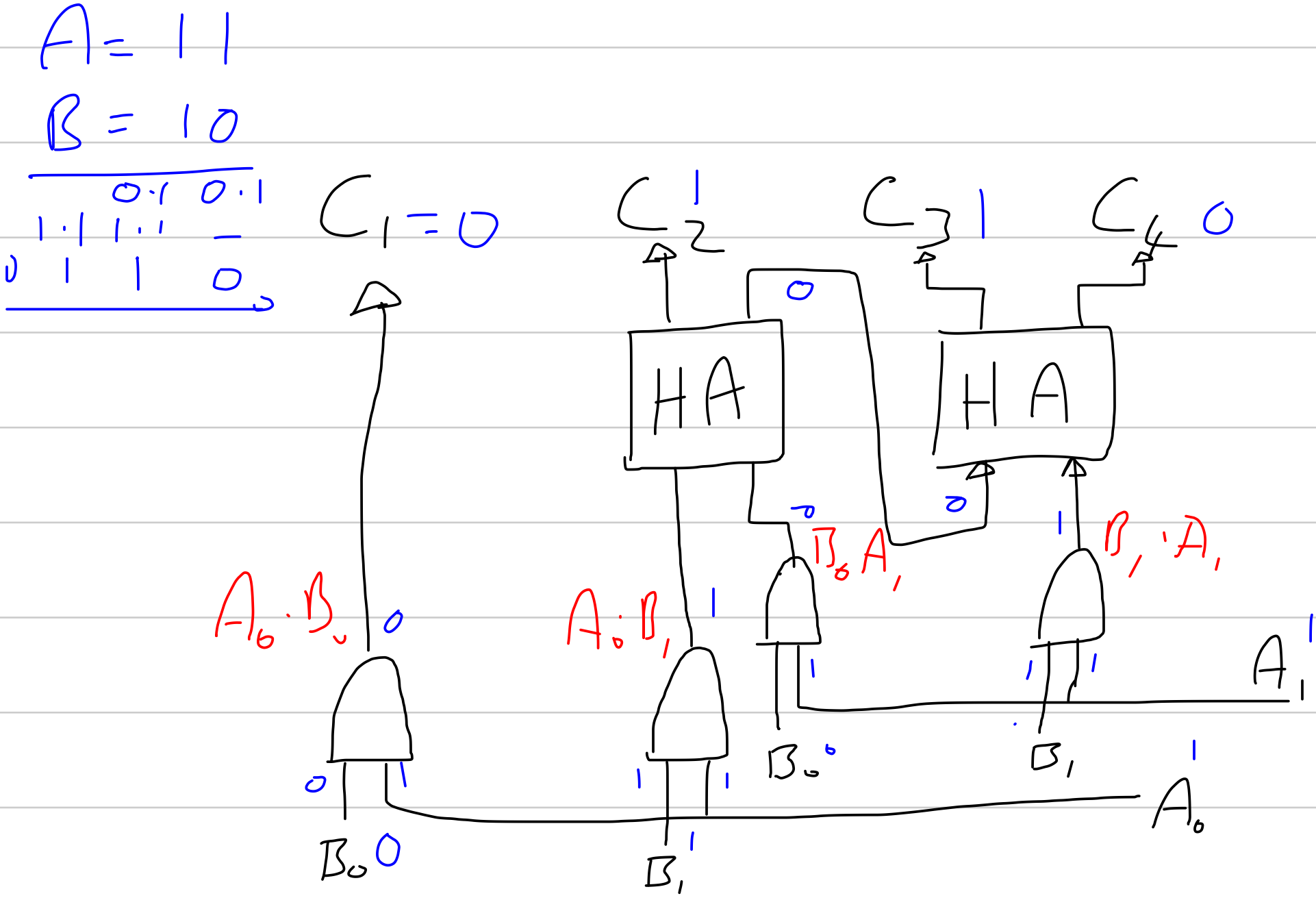
$A = 11$

$B = 10$

$0 \cdot 1 \quad 0 \cdot 1$

$1 \cdot 1 \quad 1 \cdot 1$ –

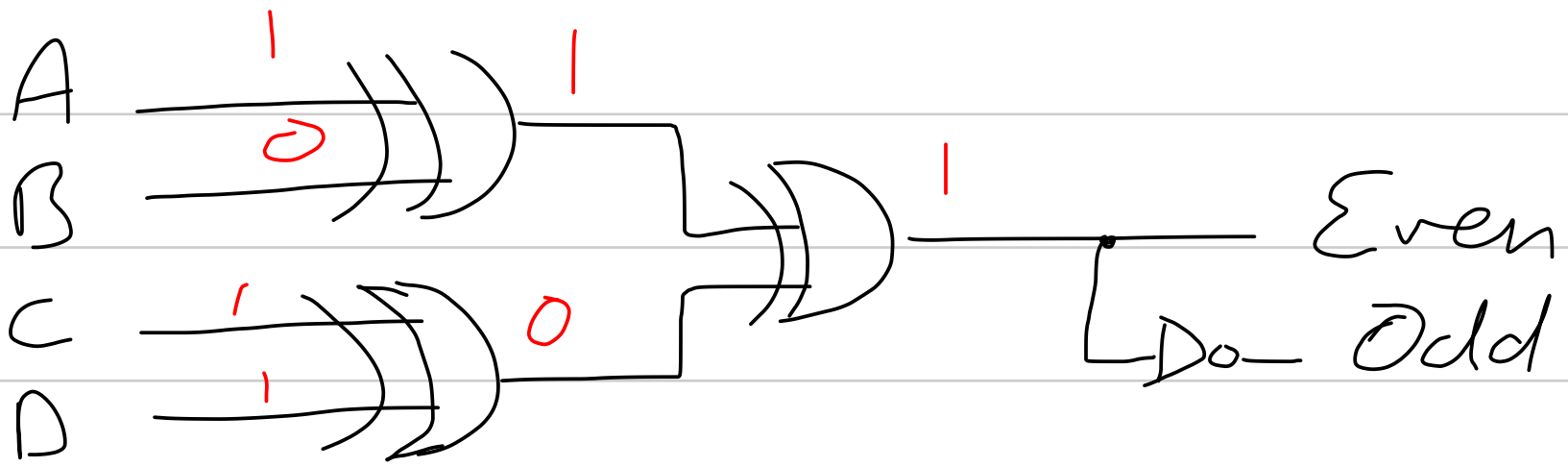
$1 \quad 1 \quad 0$



Parity bits.
Even & Odd.

1011
A B C D.

Even = 1
Odd = 0

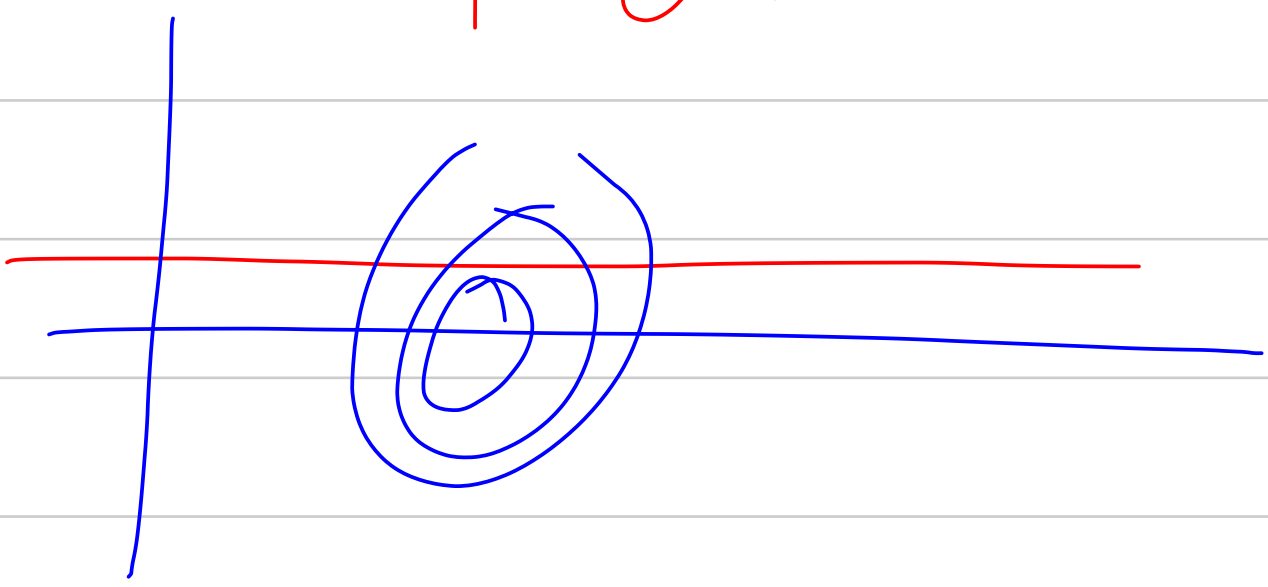


1 0 1 1

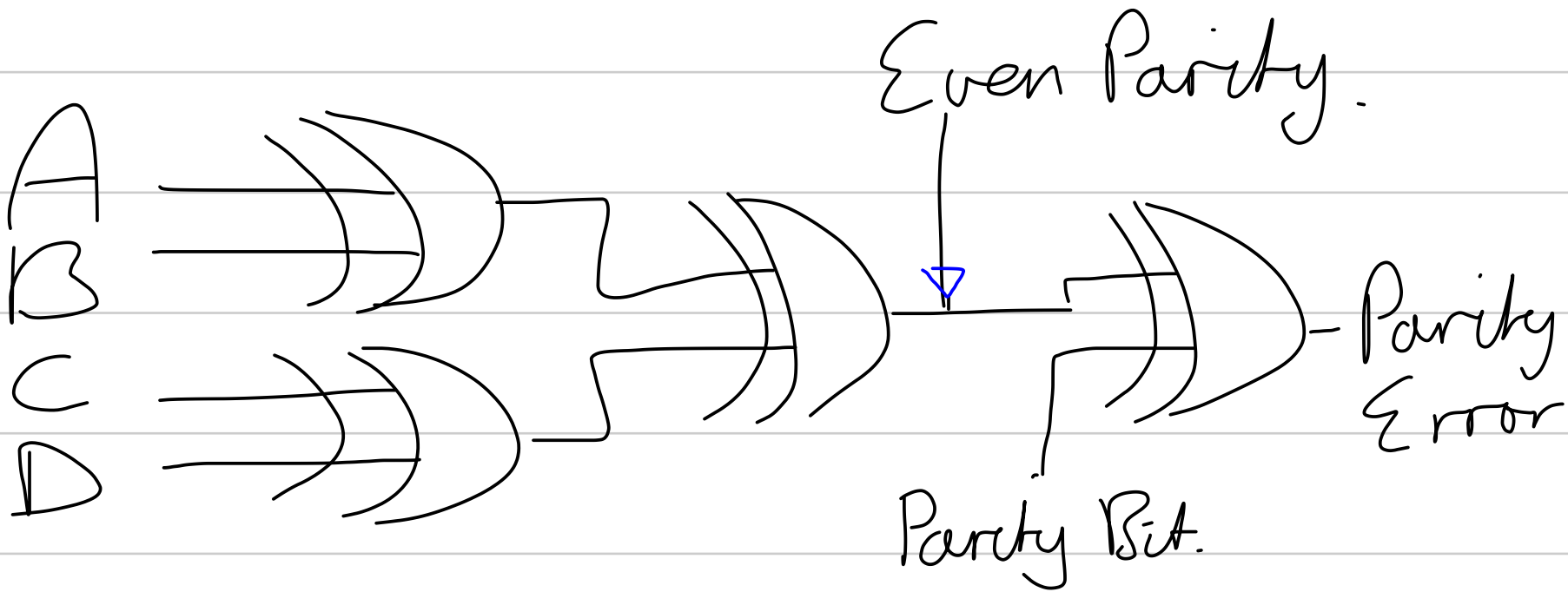
1 1 0 1

1 0 1 1 0 1

1 1 0 1 1 1



Parity checker



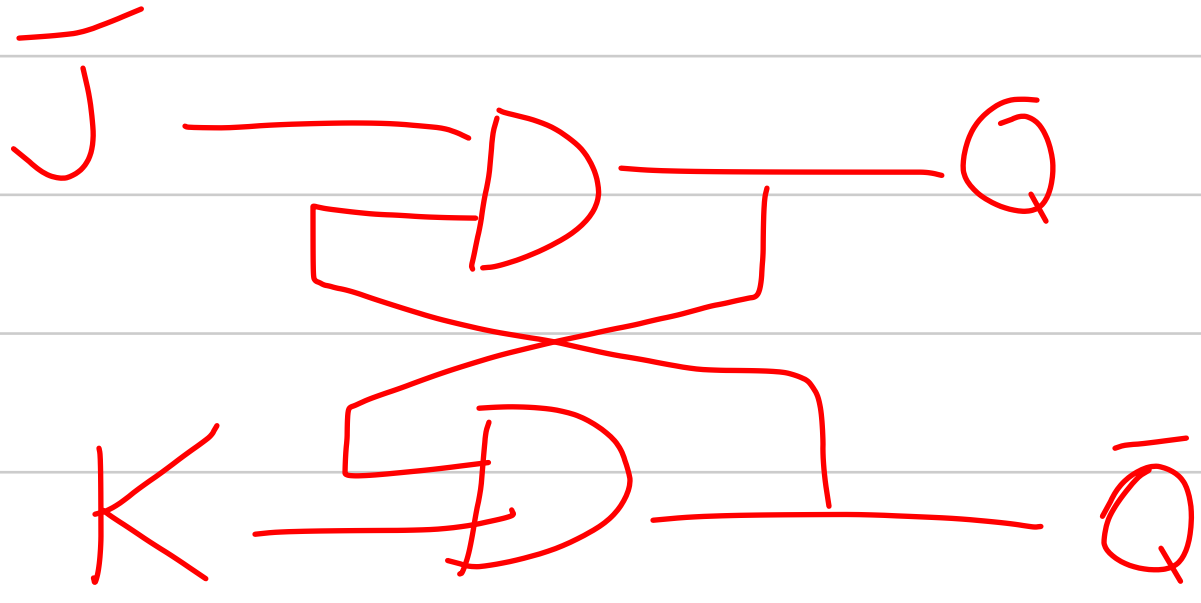
ALU → Arithmetic logic unit.

21 September 2011 – Sequential Logic

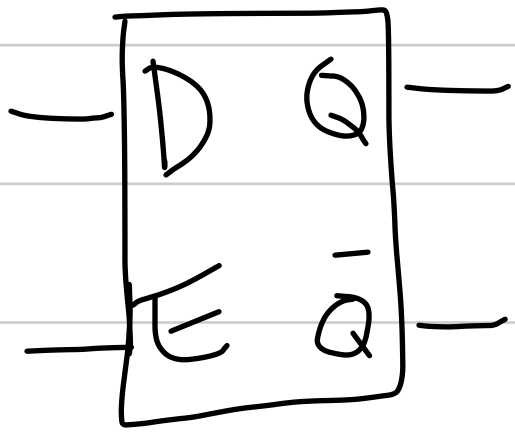
Difference between Combinational logic & Sequential logic?

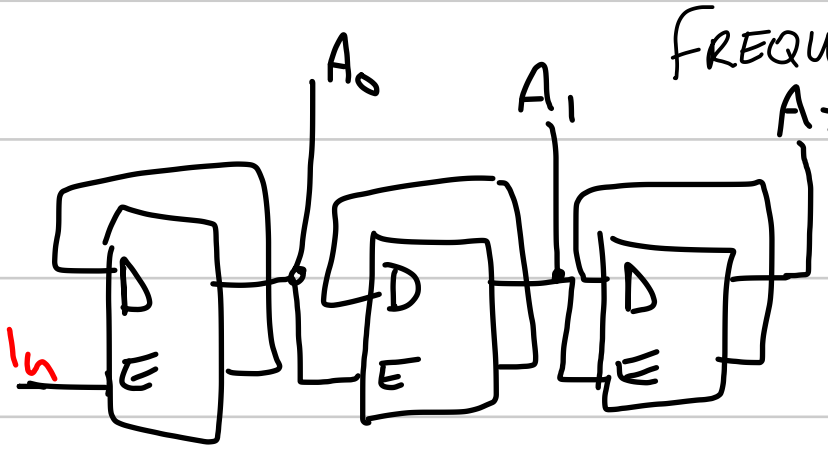
Flip-flops

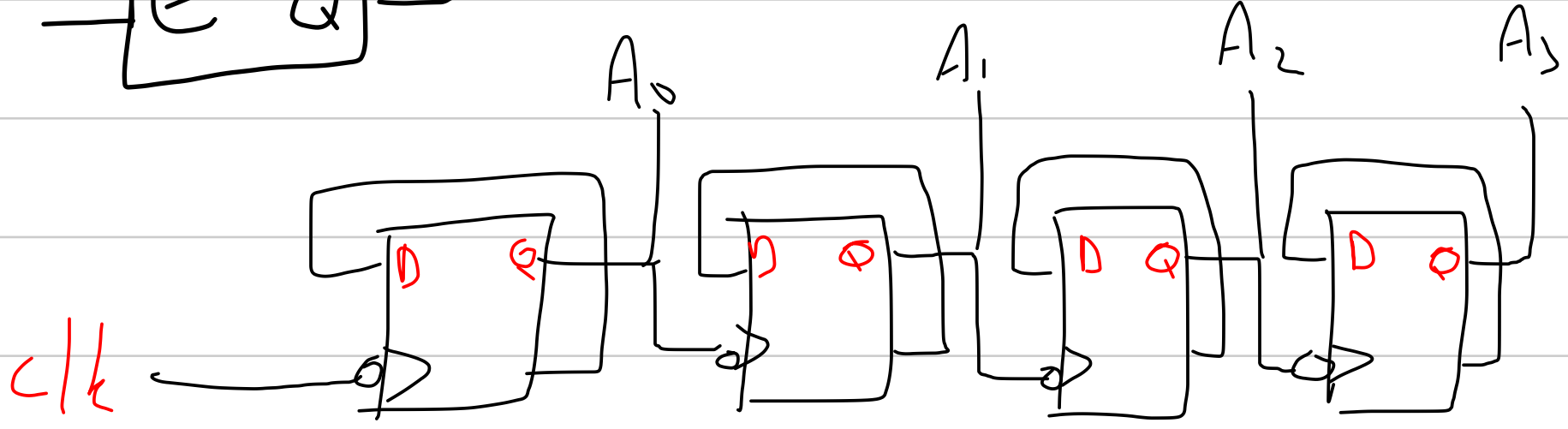
latches?

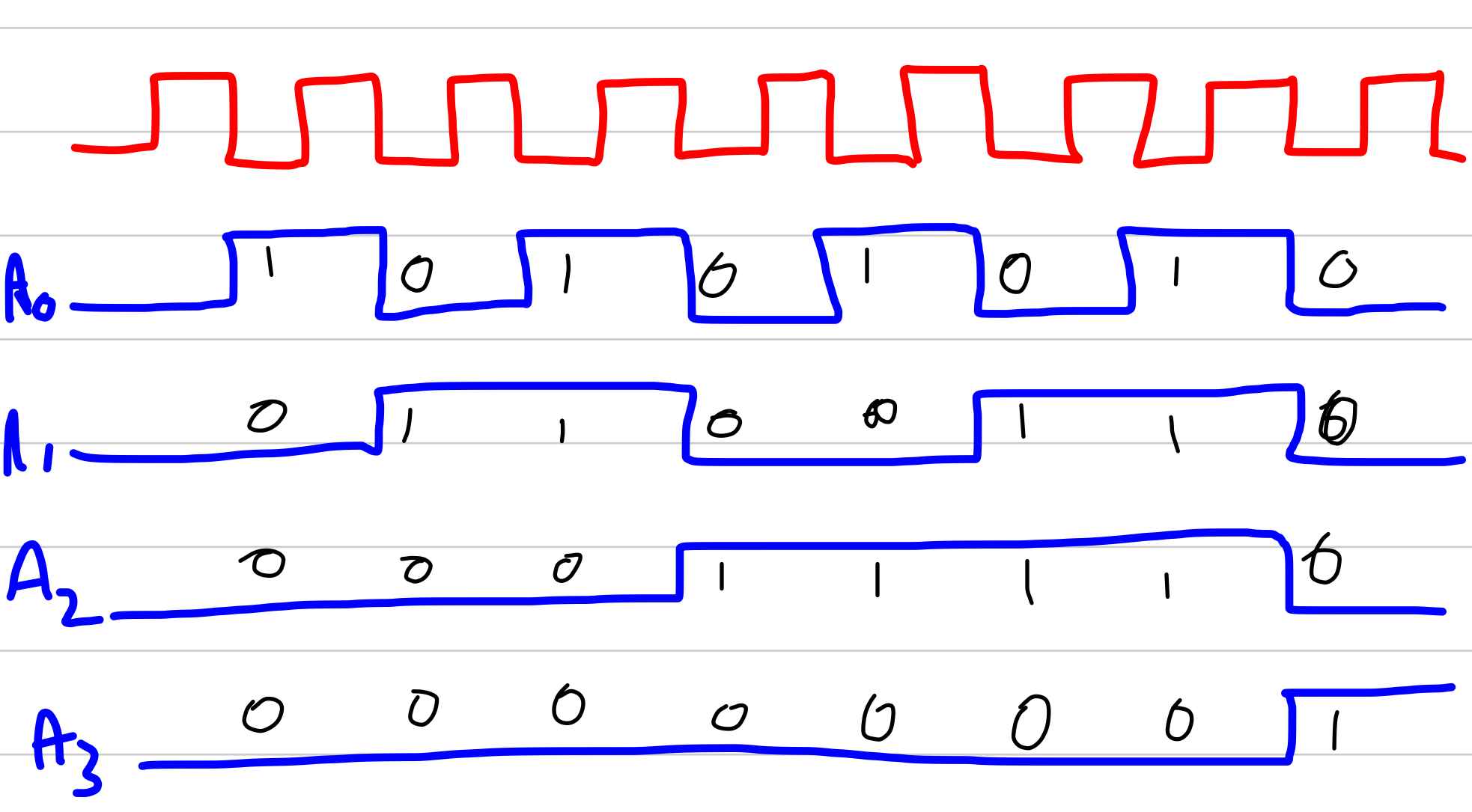


Ripple Counter



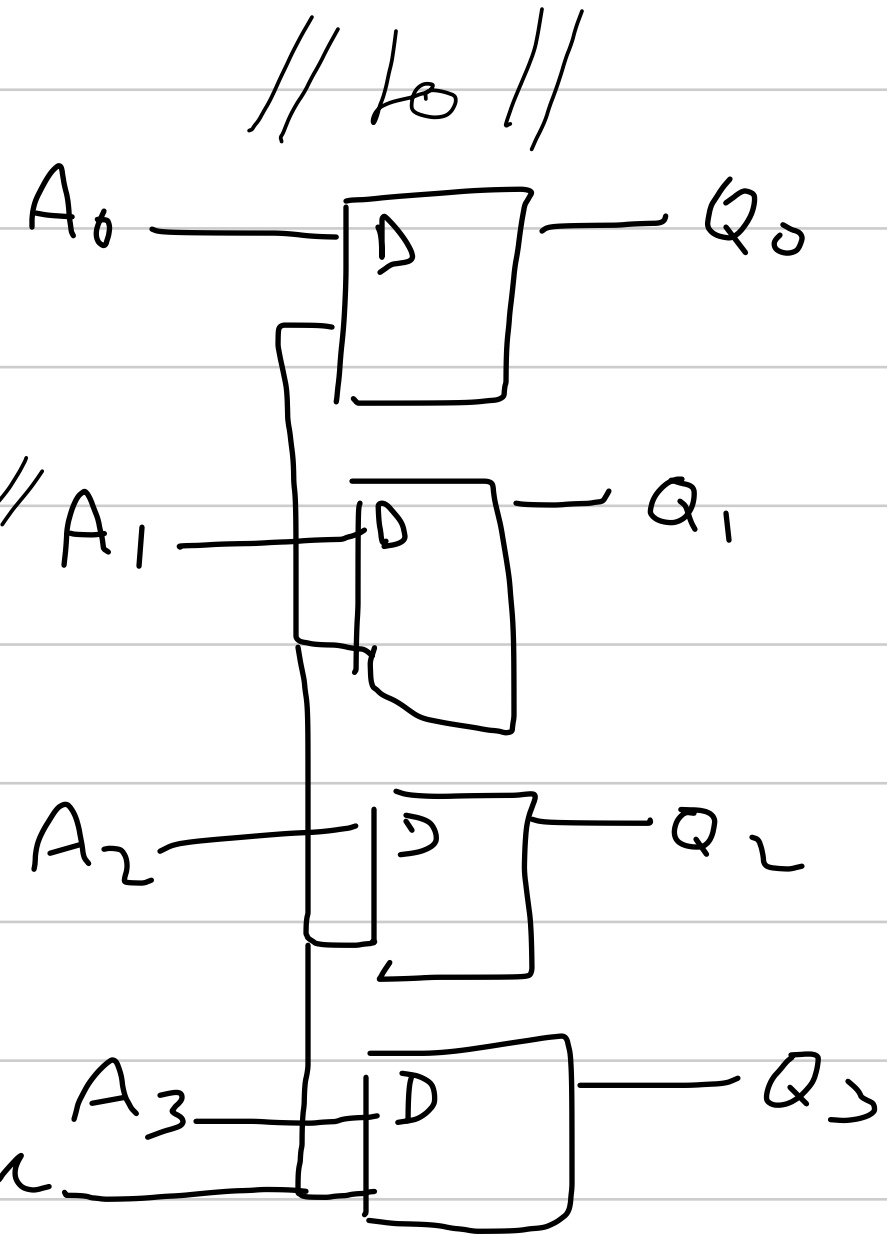




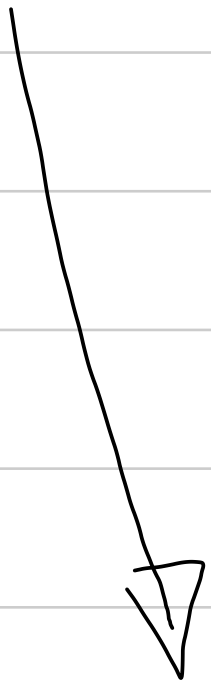


Memory / Registers

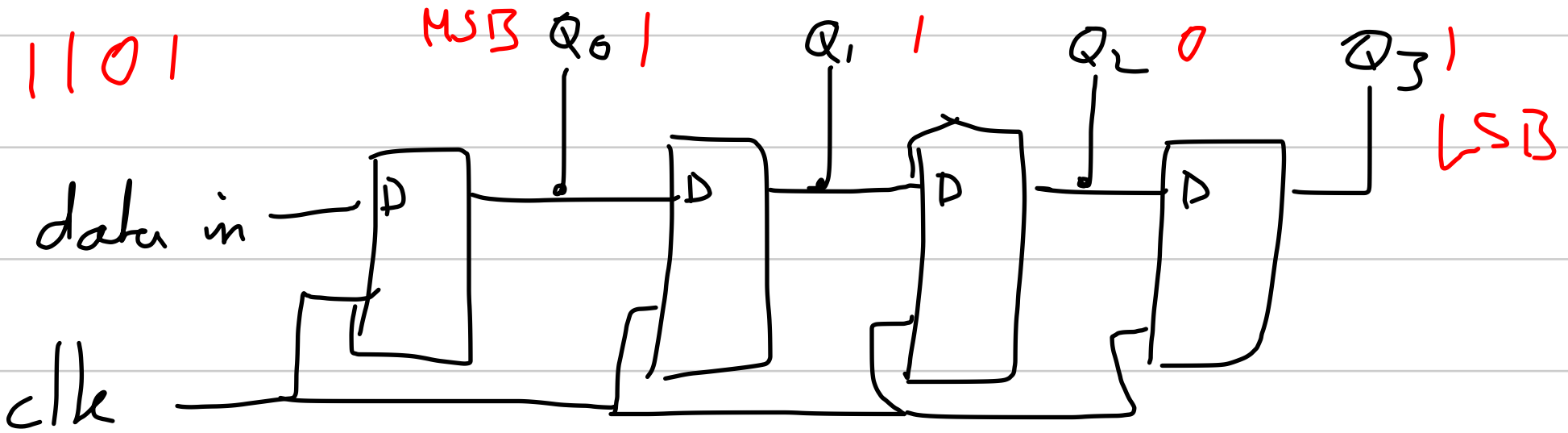
Basic memory element ?



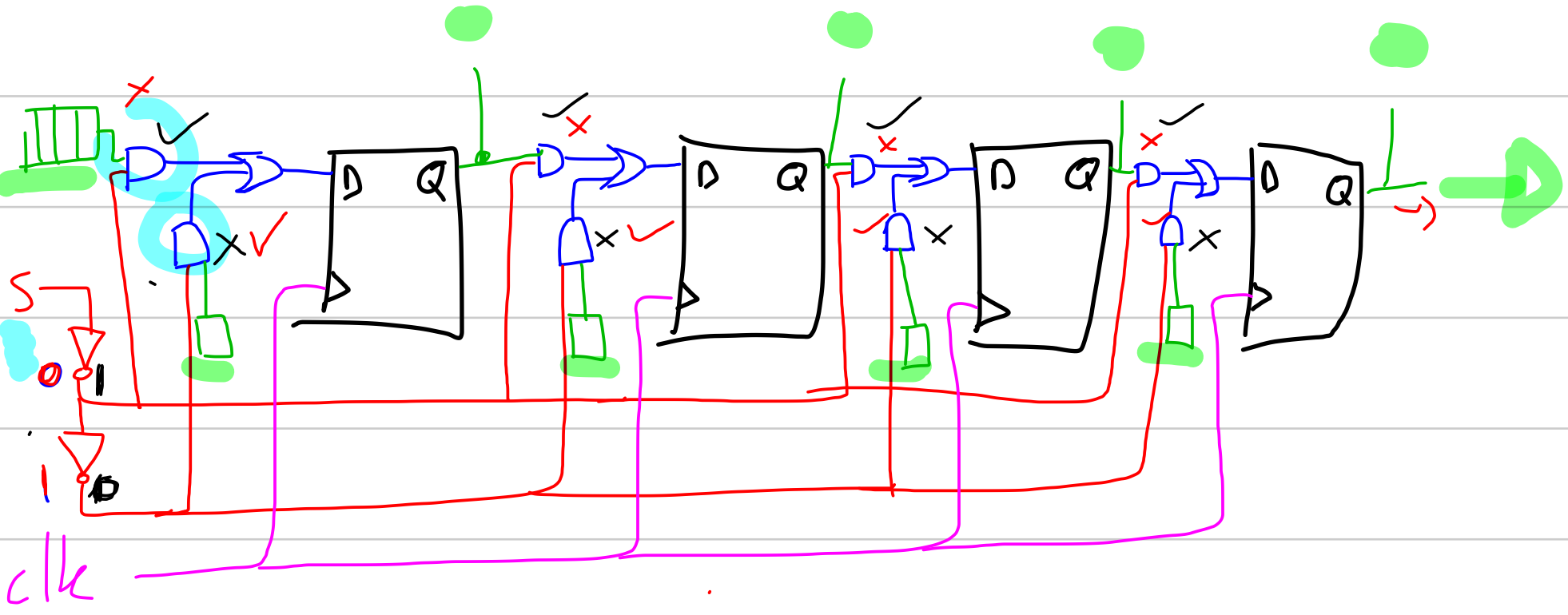
4 bit shift register! Serial to //



1101



// or Serial in // or serial out!

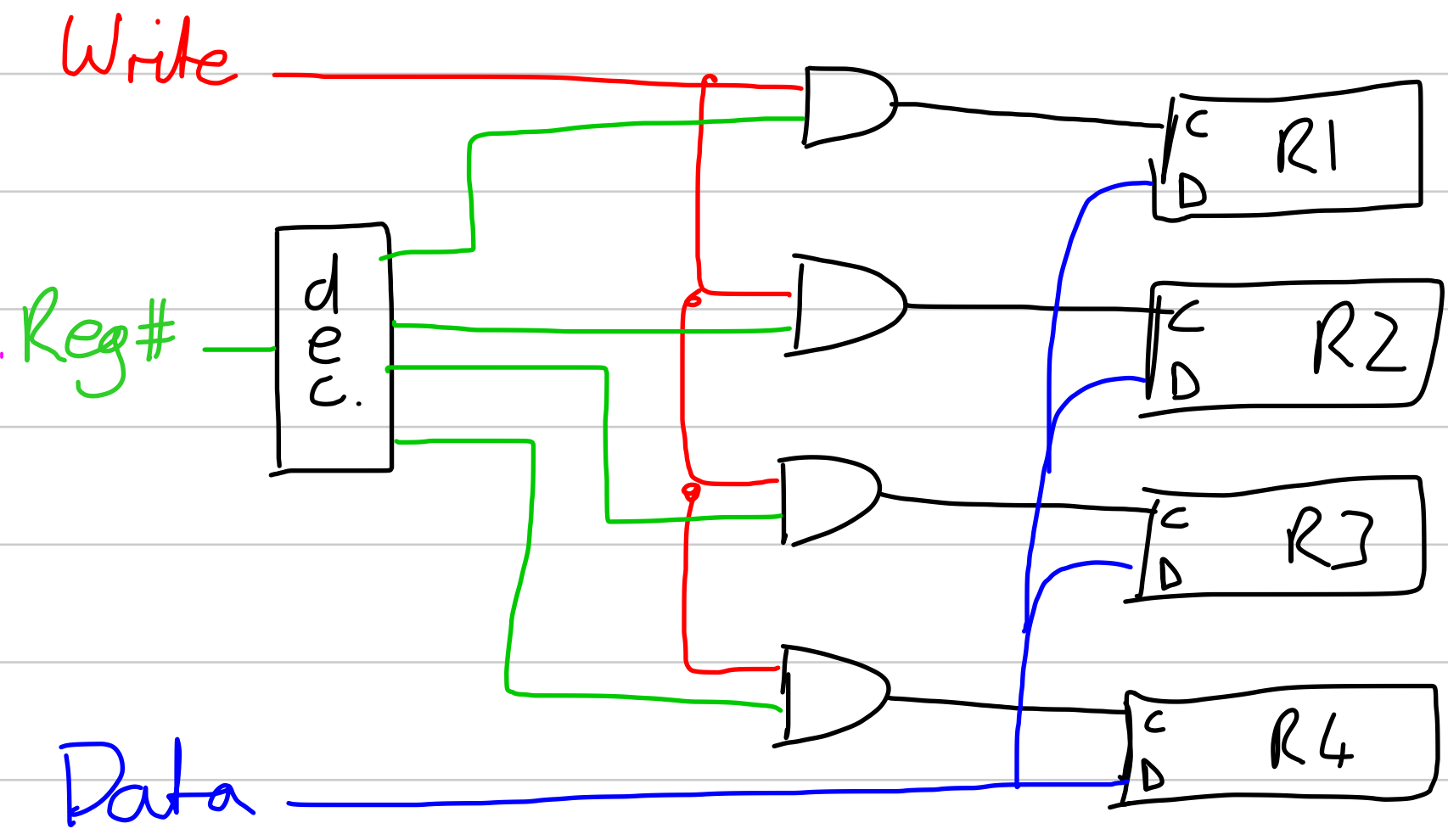


Reading registers

- Reg no
- Data
- Control

Writing to a register

- Reg no.
- data
- Clk./pulse



28 September 2011

Flip-flops - Basic memory element.

D-latch → ripple counter

Memory → // to //

→ serial to //

→ Combination: //or Serial in → //or serial out

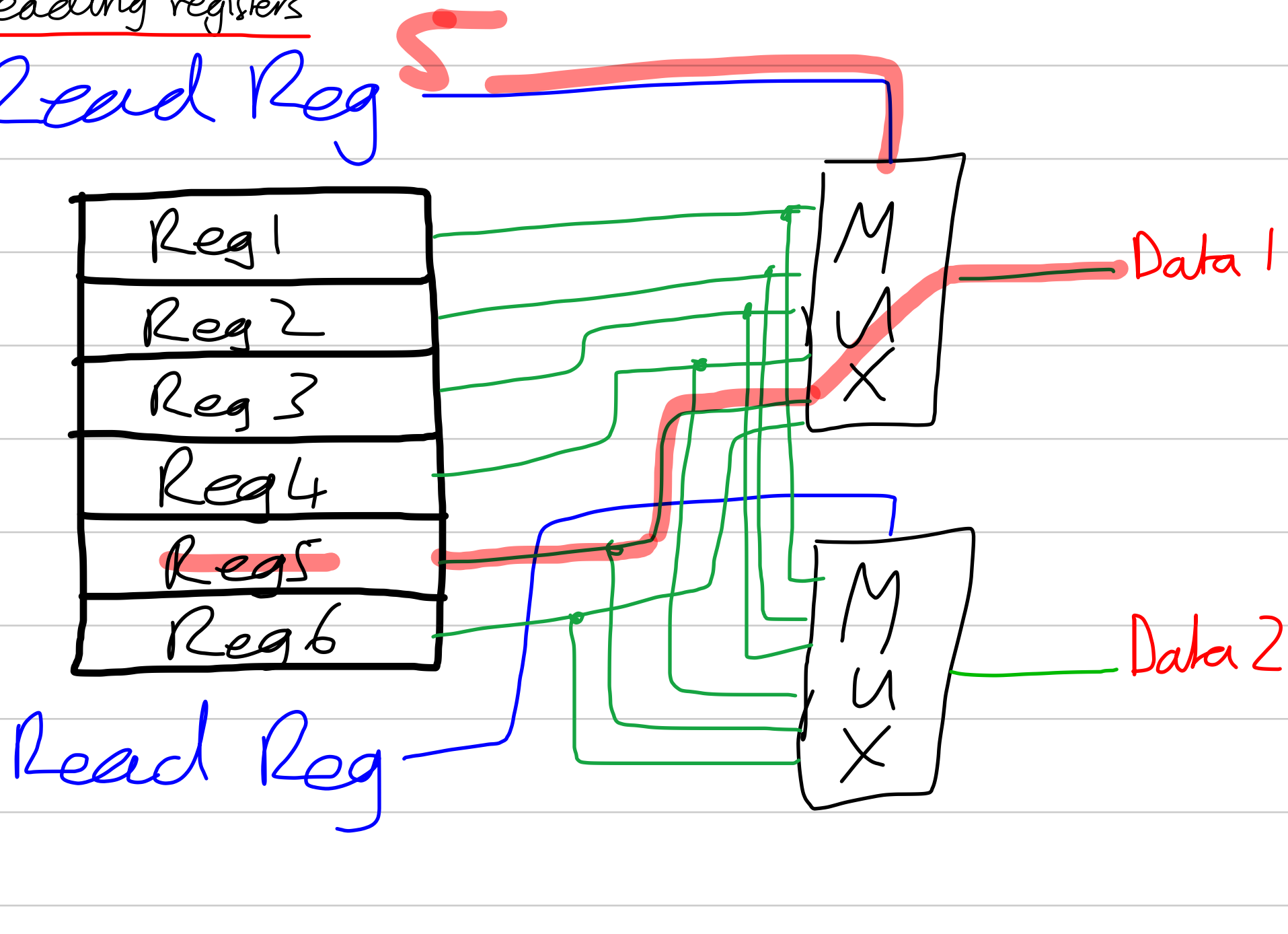
Writing registers

New → Reading registers

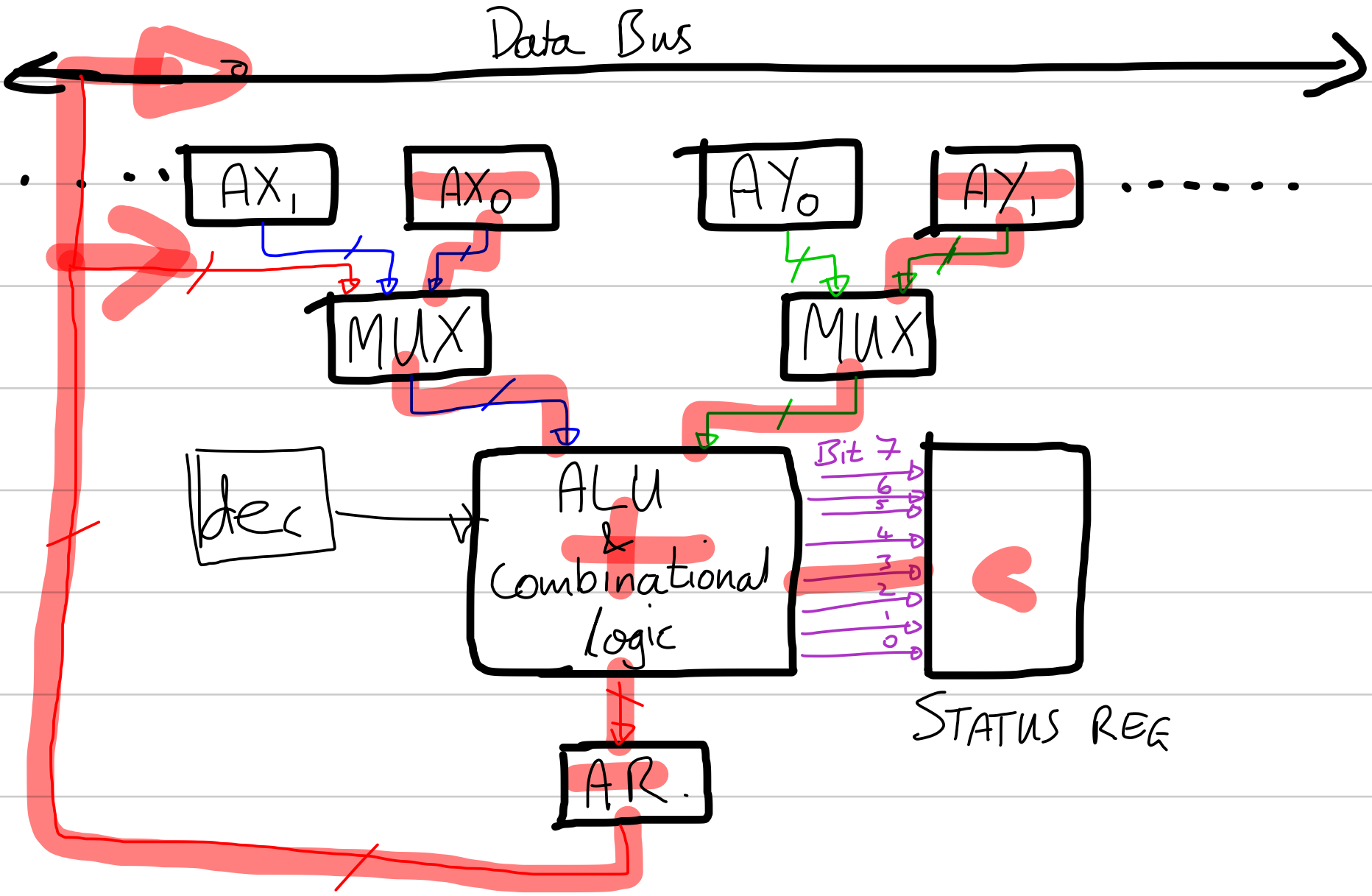
→ ALU

→ A/D & D/A converters

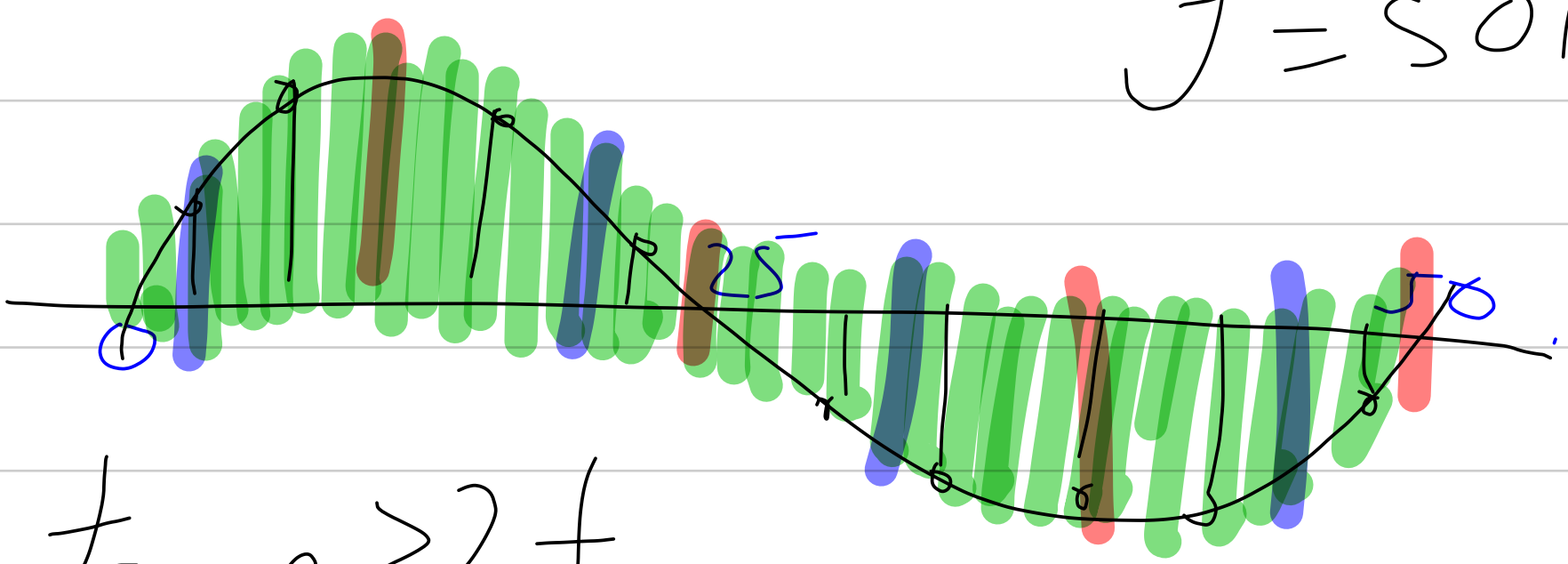
Reading registers



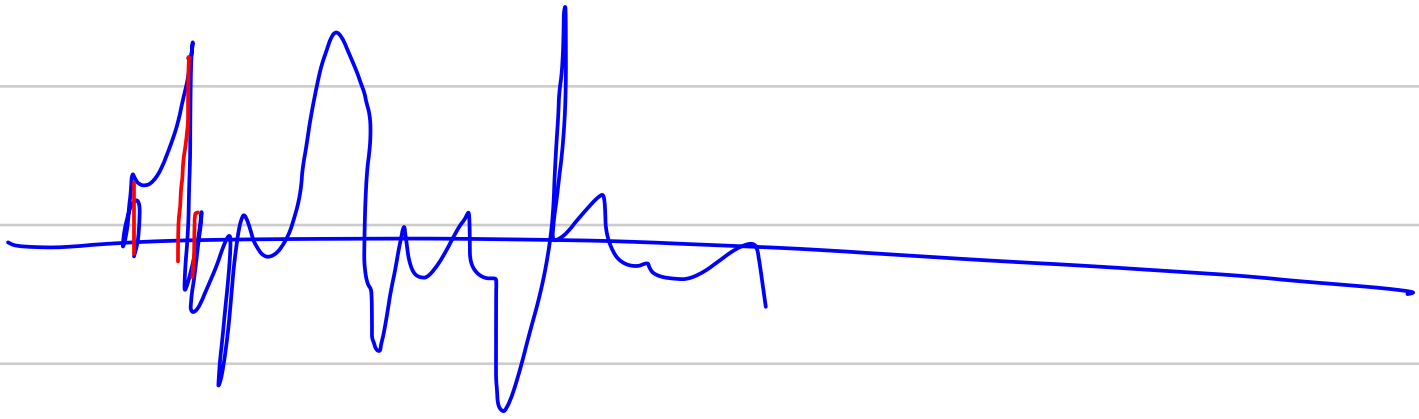
ALU → Arithmetic logic unit



A/D resolution



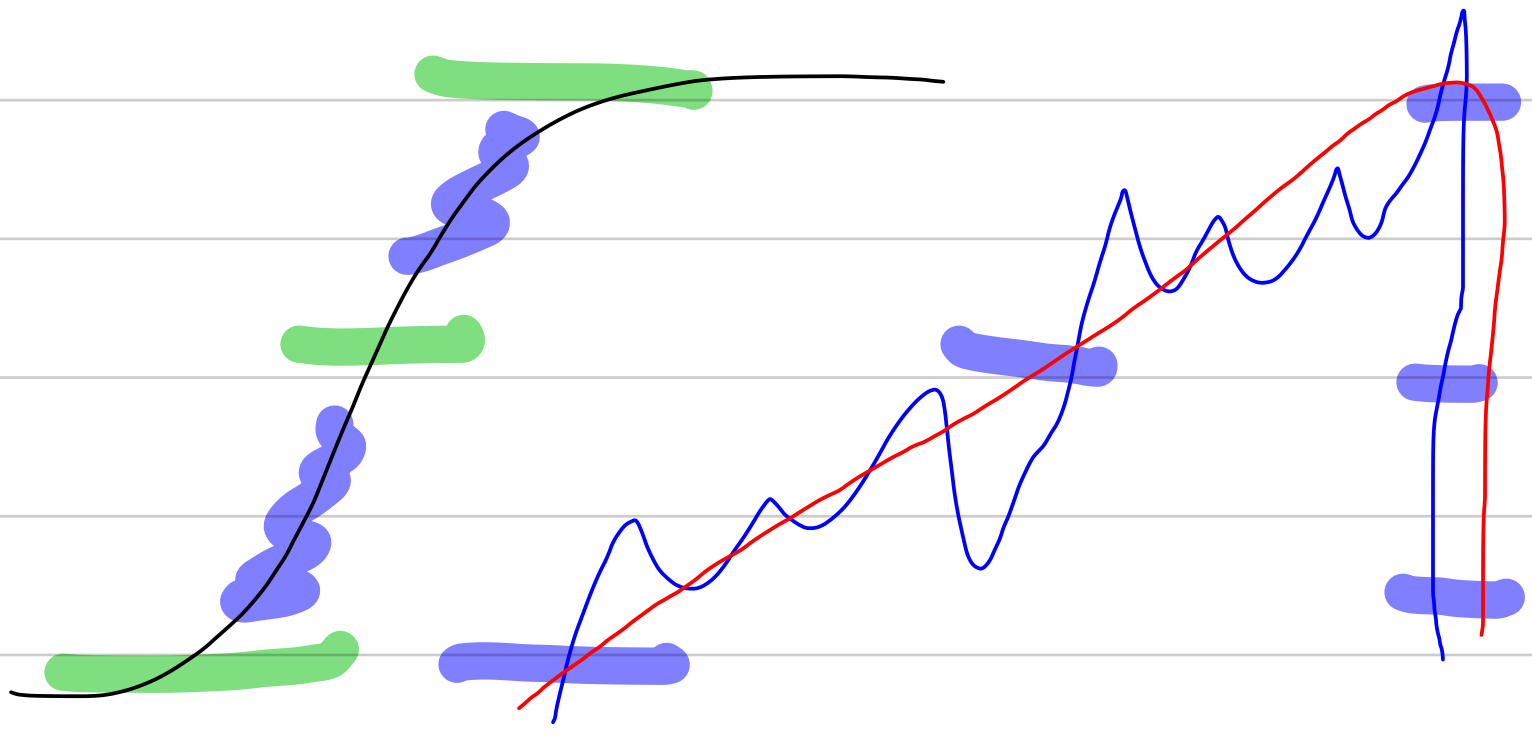
$f_{samp} > 2 f_{max}$

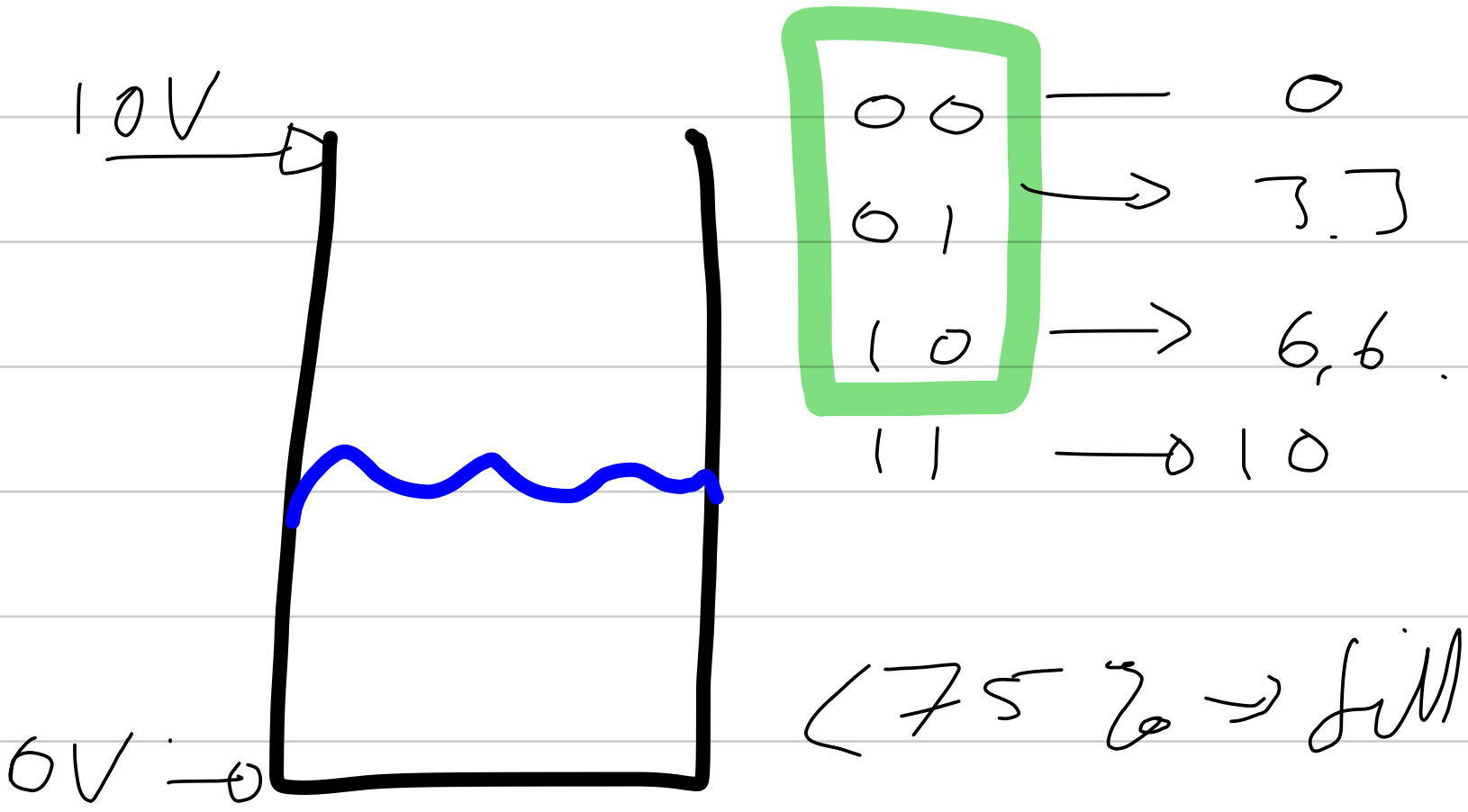


12 bits ⇒ 4096

Error ⇒ 1 / (2 × 4096)

⇒ 0,01 %





4 bits → 0 – 15

12 → 0

5 October 2011

- Reading registers
- ALU
- ADC & DAC
    - Resolution & error

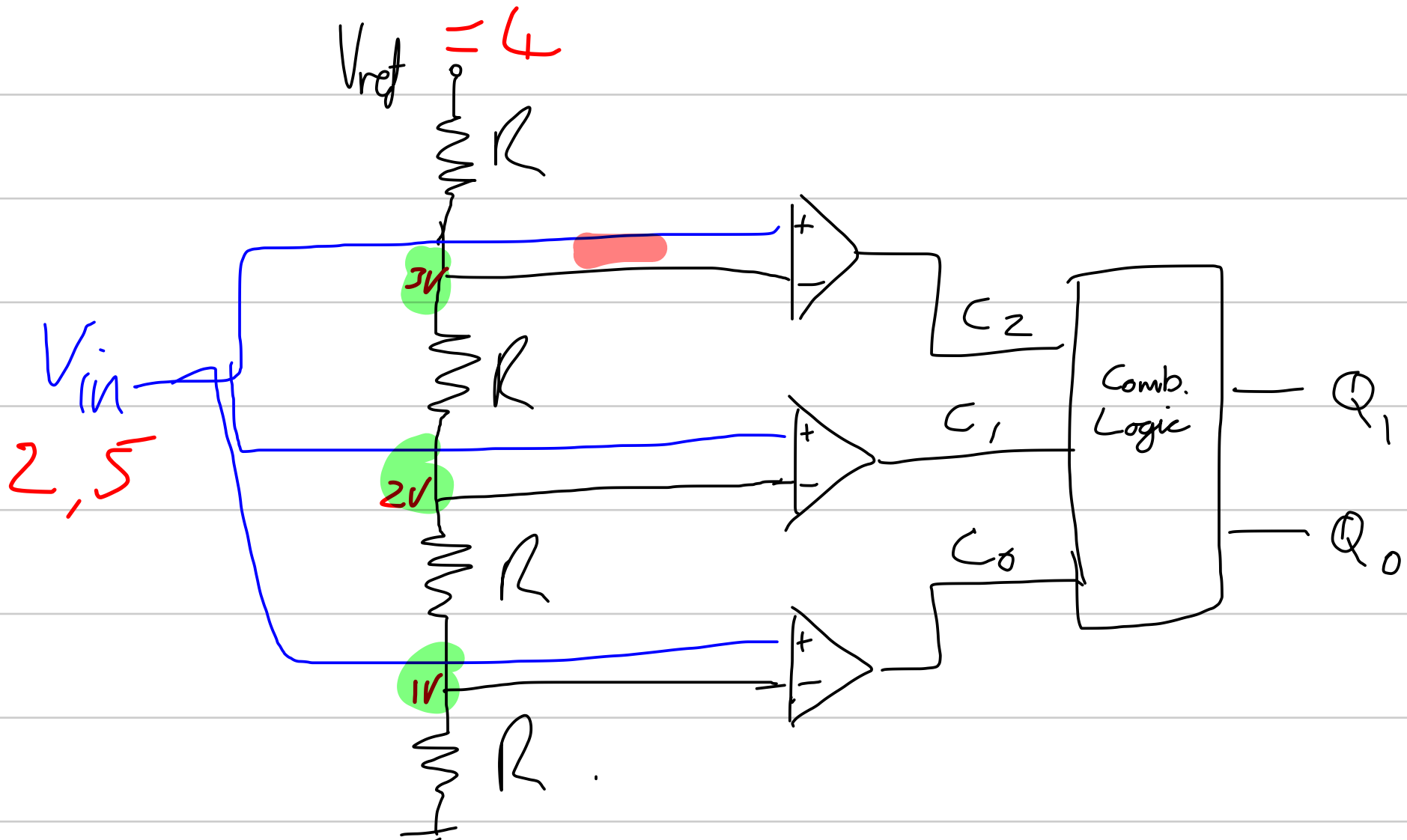
Today

- ADCs

3 Main ADC types

- Flash or parallel encoding
- Successive approximation
- Single and dual slope - already covered.

flash or parallel encoding



V_{ext} - $C_0 C_1 C_2 \rightarrow Q_1 Q_0$

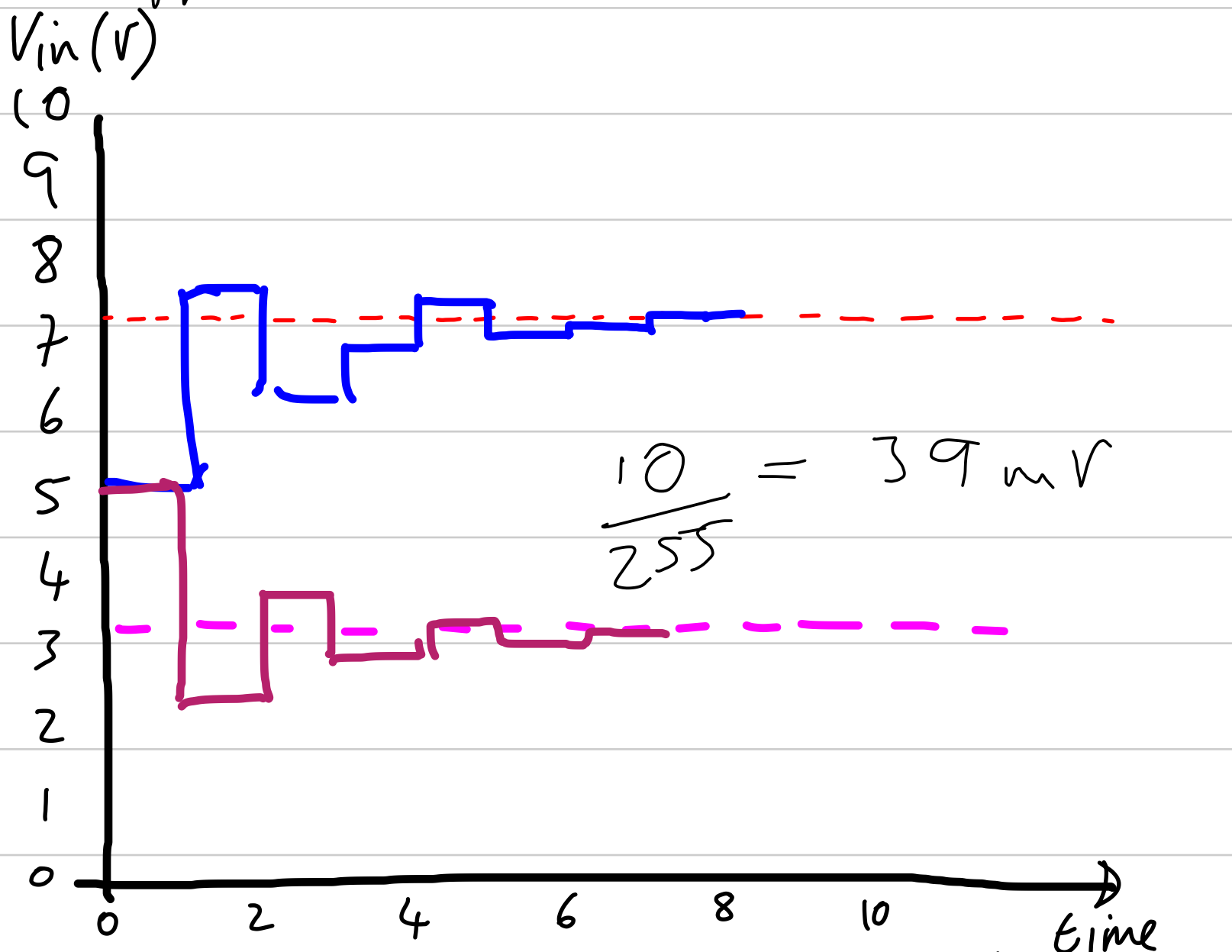
3V - 111 → 11

2V - 110 → 10

1V - 100 → 01

0V - 000 → 00

Successive approximation



$\frac{10}{255} = 39\,mV$

Resolution?

Clock cycle.	SAR bits.	Sum.	V.	Comp.
0.	01111111.	127.	4.98.	Too small
1.	10111111.	127+64=191.	7.49.	Too big
2.	10011111.	191-32=159.	6.24.	Too small